UPDATE TO DESCRIBE POTENTIAL APPROACHES FOR DEALING WITH VDLM2 INTERFERENCE (AIR AND GROUND)

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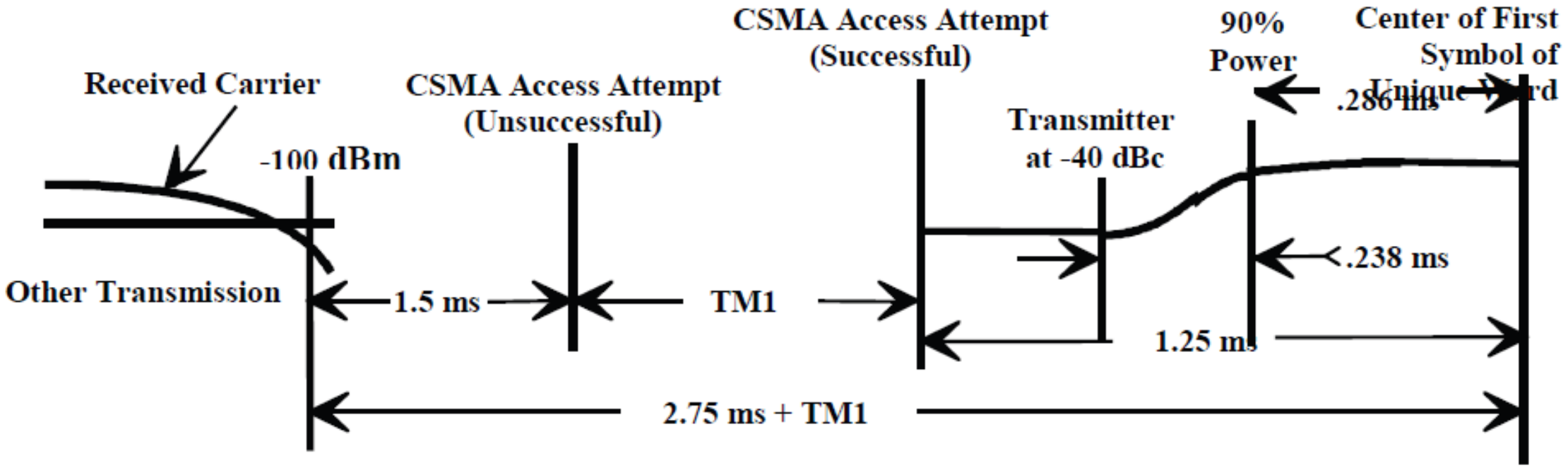
OPTIONS TO IMPROVE CSMA NOISE REJECTION WHILE REDUCING IMPACT TO POTENTIAL VULNERABILITY TIME OF P-PERSISTENT CSMA

1) **Add SYNC (PREAMBLE) detection to CSMA logic**
   - Introduces the minimum additional delay to the current implementation with minimal impact to the VDR (uses already available logic in current implementations).
   - May introduce an additional delay between 0.48ms (assuming channel was not already busy, and the power rise is due to the SYNC/PREAMBLE) and 1.48ms (assuming channel was already busy)
2) **Add the presence of valid D8PSK modulation to CSMA logic**
   - The added delay, if any, could be considered negligible as it would be part of the same signal processing that occurs while calculating channel power and SYNC/PREAMBLE detection (including symbol clock detection/synchronization).
   - Requires changes to the current VDR logic (may only be feasible to implement on newer VDR architectures)

We need to keep in mind that any change must be a compromise to improve the CSMA performance against wideband noise while reducing any practical impact on message collisions of real (not theoretical) installations

Bottom line – reduce any additional time added to current CSMA logic

DO-224 CSMA TIMINGS

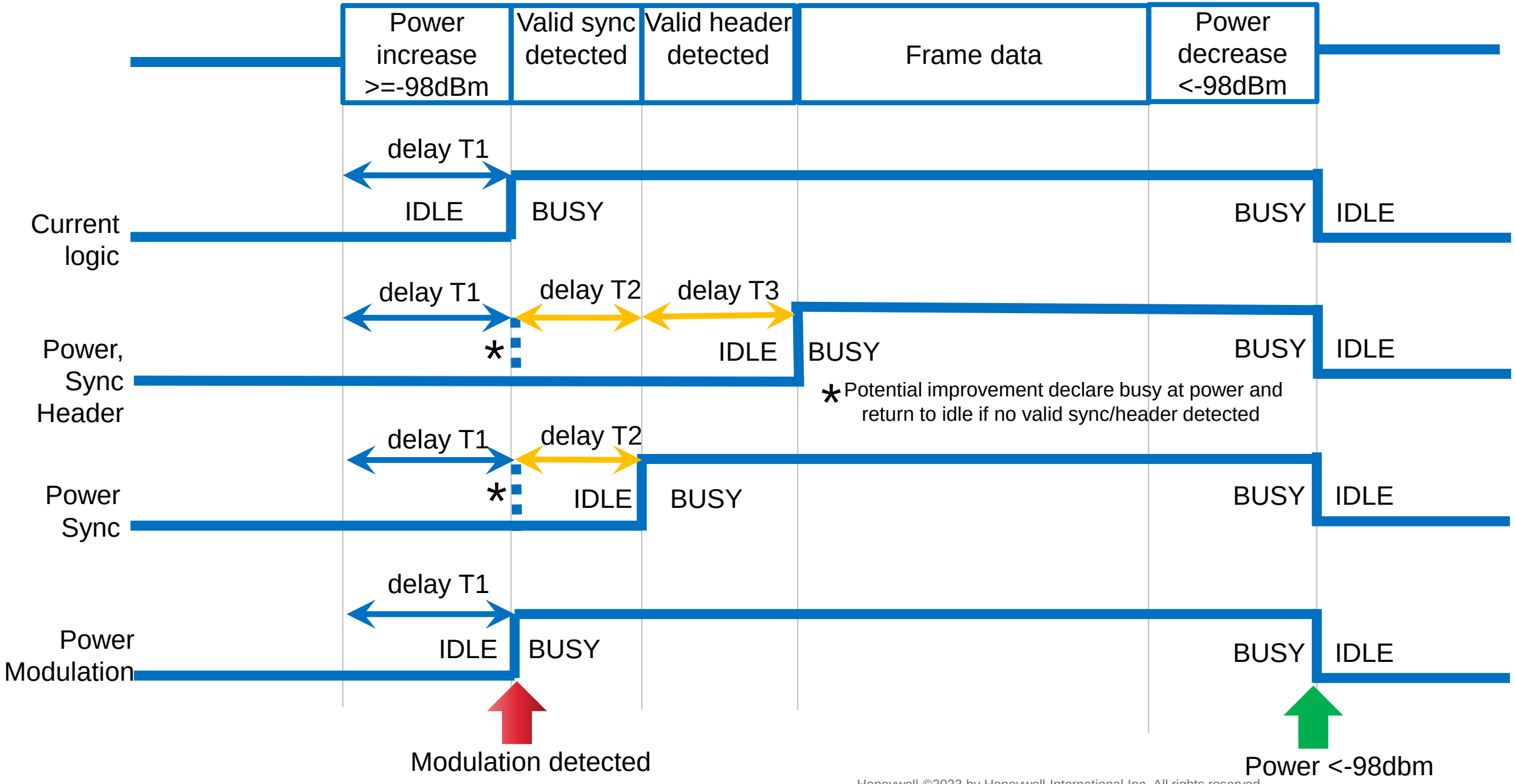


TM2 (Channel busy) = 120 seconds.

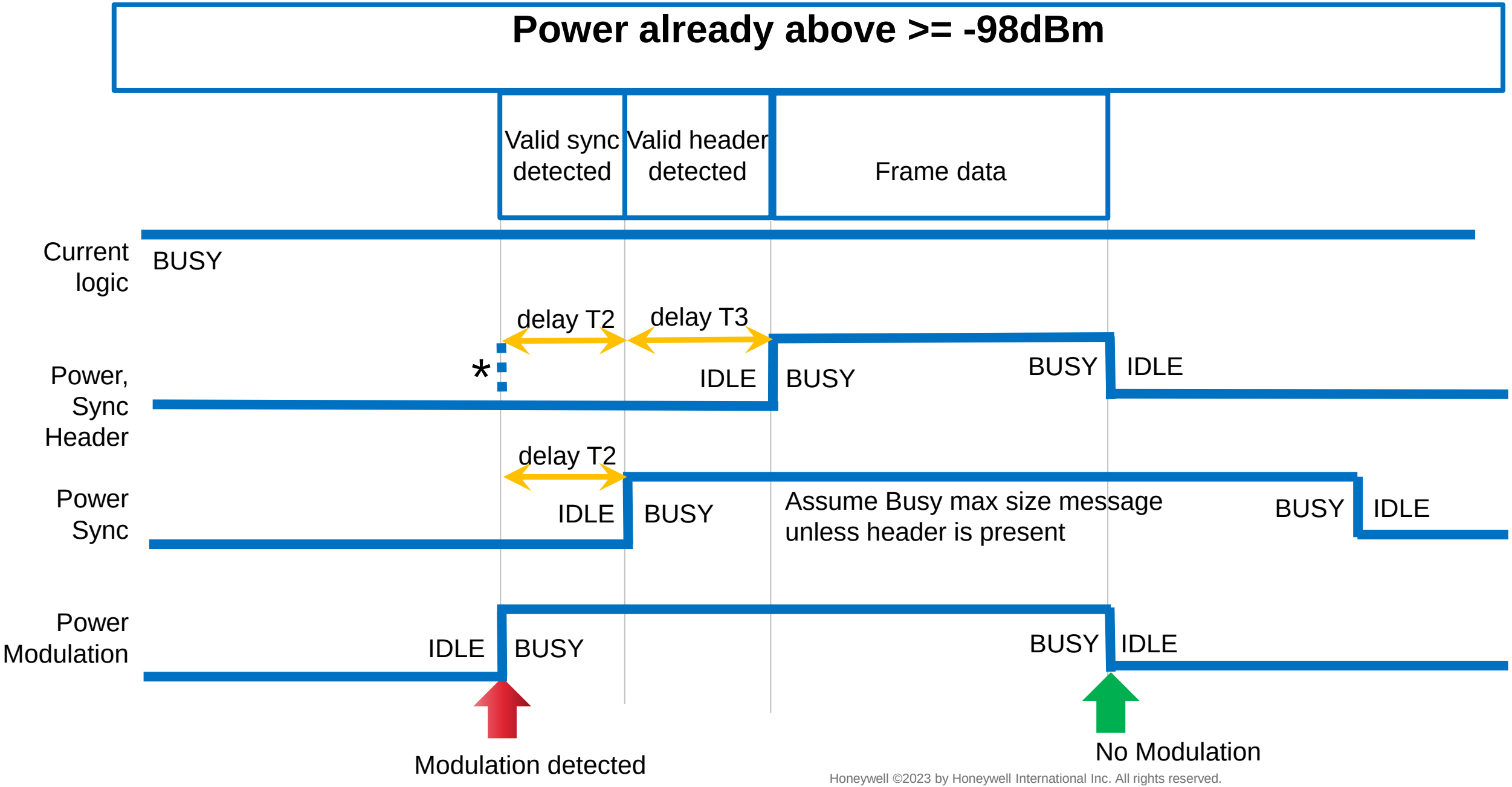
p (Persistance) = 1 (256/256)

M1 (Maximum no. of attempts) = 65,535

DETECTING CHANNEL BUSY WITHOUT NOISE



DETECTING CHANNEL BUSY WITH NOISE



SUMMARY

- **3 alternatives to current channel busy sensing logic add ability for transmissions during interference conditions.**
  - Power with additional sync and header detection adds additional vulnerability for the time it takes to detect the sync(T2) and header(T3), especially during interference condition.
  - Power with only sync detection adds vulnerability for the time it takes to detect the sync(T2), especially during interference condition. Reduced by T3.
  - Power with modulation detection does not add vulnerability during interference condition.

BACK-UP SLIDES

D8PSK CHANNEL POWER OR RAW CHANNEL POWER + D8PSK MODULATION PRESENCE

What about changing detection logic from:

- If the detected on-channel power rises to at least minus 98 dBm +/- 2 dB for at least 1ms; the Channel will be considered BUSY

to:

- If the detected on-channel power from valid D8PSK modulation rises to at least minus 98 dBm +/- 2 dB for at least 1ms; the Channel will be considered BUSY

Or

- If the detected on-channel power rises to at least minus 98 dBm +/- 2 dB for at least 1ms AND valid D8PSK modulation is detected; the Channel will be considered BUSY

Leave it to Equipment Manufacturers to define how to detect valid modulation

This is similar to Option 4 from the original SC-214 questionnaire