1.0 INTRODUCTION

This standard describes the aircraft Electronic Flight Bag (EFB) interface from the perspective of the aircraft signal interface to the flight deck, typically installed as one or more physical connectors. The intent is to provide a standard interface between a general purpose computing device installed as an EFB, and factory installed avionics equipment.

COMMENTARY

This commentary is provided to help those readers not directly involved with ARINC 828 development understand some of the reasoning behind the decisions made in selecting the connector and wiring configuration presented within this standard. Given that an EFB installation interface may vary from just a few simple interfaces to an installation with many complex interfaces, a scalable standard was written. Therefore, this standard specifies the use of conductors (wire and cable types) that will accommodate a wide range of signal types. Multi-use signal pins are also specified within ARINC Specification 828.

To provide a connector arrangement that does not burden installations requiring minimal aircraft interfaces with a large and expensive connector, it was decided to specify a connector configuration that would support a building block approach. This approach allows the integrator to select and install the required subset of connectors identified within ARINC 828.

To ensure the best quality signal path integrity, the Quadrax contact was selected for use with the more sensitive signal types such as video signals (LVDS and DVI). The use of the Quadrax contact provides numerous benefits among which are:

- Controlled impedance carried through the full length of the video cable link
- Ability to maintain consistent shielding through the full length of the video cable link
- Supports modular fabrication of the video cable bundle for implementations that require a non-standard, or sensitive, Quadrax contact termination technique, the assembly operation can be performed off the aircraft in a controlled environment
- Provides the ability to create preassembled Quadrax wire segments that can be routed individually in a retrofit aircraft installation

To accommodate a multiple connector configuration that provided the Quadrax insert option and had multiple sources available, the Mil-Std 38999 connector series was specified.

1.0 INTRODUCTION

1.1 Scope

This standard was written to define:

- Common connector(s) that are installed in or near the cockpit by the airframe manufacturers at the time of aircraft production or by the aircraft owner/operator during an EFB retrofit
- A set of interface services intended for a general purpose computing device (e.g., EFB)

The objective is to support typical EFB system installation and EFB software applications intended for forward fit and retrofit installations.

1.2 Benefit

This standard is expected to minimize the overall cost to equip an aircraft with an after-market EFB that may utilize a variety of general purpose computing devices and an Aircraft Interface Device (AID). The definition of a common connector and wiring interface provides numerous cost savings benefits such as:

- Allowing the development of standard AID interface hardware and interface cabling
- Providing economies of scale for the AID products and interface cabling
- Reducing engineering and installation costs, and aircraft down time when installed at the factory
- Reducing engineering definition effort related to retrofit installations
- Allowing use of common EFB equipment across multiple aircraft

1.3 Definitions

Acronyms and terms uniquely associated within this document are described below.

1.3.1 Aircraft Interface Device (AID)

The AID is a device or function that provides an interface between the EFBs and other aircraft systems which protects the aircraft systems and related functions from the undesired effects from non-certified equipment and related functions.

An AID may be implemented as a physical device, e.g., a docking station that combines the above mentioned characteristics to other functions, such as EFB equipment mechanical mounting, data storage or routing, power conditioning, and others.

The AID may convert aircraft-specific signals to those commonly used in EFB equipment. In no circumstances should the behavior of the AID cause adverse affects to the aircraft. As such, the AID must meet all applicable regulatory requirements.

1.3.2 EFBPU (EFB Processor Unit)

As used within this document, an EFBPU is only used for its processing capability. For example, it may be an aviation-grade computing device without terminal hardware, or it may be a laptop computer or similar device which terminal functions are deactivated or unused while docked.

An aviation-grade computing device may contain the AID or portion of the AID. Possible terminal functions are not used.

1.3.3 Terminal

Used within this document, a terminal is any human interface device that enables the user to control the EFB system (e.g., display, function keys, keyboard, touch-pad, touch-screen, or mounted USB Ports).

1.3.4 Network Server Unit (NSU)

From the perspective of the EFB, the NSU may provide common data/file storage, open systems processing, and network communication to EFB devices.

The form and fit is defined in ARINC Characteristic 763A. The functions provided are defined in ARINC Report 821. Legacy form, fit, and function are defined in ARINC Characteristic 763-3.

1.4 Implementation

Appendix C contains Example Use Cases identifying possible configurations for the EFB, the AID, and associated aircraft connectivity options. They typically vary depending on available aircraft provisions (terminal, EFBPU, switches) and operators' EFB implementation objectives.

The Example Use Cases are neither prescriptive nor limitative in nature. They are provided to suggest possible applications of this Specification. In these cases, the AID is represented in various suggested configurations. The cases also identify to possible ways of using the connectors J1 through J7.

The Example Use Cases do not intend to imply the use of any specific EFB Class as defined in AC120-76a.

Appendix L defines the RFB Terminal Interface using Ethernet and Remote Frame Buffer (RFB) protocol.

1.5 Compliance

This section describes what the aircraft manufacturer must do to claim compliance with ARINC Specification 828. Several levels of compliance are defined. The following statements are intended to represent what is needed for commercial compliance, in addition to what is needed to assure regulatory compliance. ARINC documents do not specify regulatory requirements.

Because the aircraft installation will utilize transition cables that convert the EFB hardware connector to the ARINC 828 standard interface at the reference plane (P1 through P5), hardware such as the EFB Processor Unit and AID are not required to have specific connector types in order to claim ARINC 828 compliance. Connector definition on this EFB hardware is outside the scope of ARINC Specification 828.

Level 1 compliance

To claim ARINC 828 level 1 compliance an aircraft should provide at least two ARINC 828 J1 connector receptacles in or near the cockpit. Through these connectors and in accordance with the relevant sections of ARINC Specification 828 the aircraft should provide to the EFB:

- EFB identification discretes (EFB_Disc2-A, EFB_Disc2-B)
- EFB shutdown signal (EFB_Disc3)

- Power
- Ethernet inter-connection between at least the J1-Eth4 port from at least two J1 connectors
- J1 connector should have wires attached to all connector pins. Except:
  - If only one power source is available, then no wire is needed for the unused power pins.
  - Aircraft discrete pins with assigned functions which are not supported by the aircraft type may be left unwired
  - Quadrax insert A (USB_1) may be left unwired if J3 exists in a given installation and either J3 Quadrax insert K (Eth_2) or J3 Quadrax insert A (Eth_3) is wired.
- All wires attached to all connectors must meet the signal standards specified in Section 2.1.1, Digital Signals, Appendix A, Standard Wire Types, and the airframe manufacturer's wiring specification. The routing of the wiring is not specified in ARINC Specification 828.
- Wires from an ARINC 828 J1 through J5 connector may end at a non-standardized connector at an installed LRU, at a backplane of a rack provisioned to carry an LRU, or stowed at a designated point for future use. The location and characteristics of this point of stowage is aircraft specific, but it should be at a location where the airframe manufacturer foresees aftermarket installation of equipment.
- There should be one or more switches, reachable from at least one pilot seat, through which power to all J1 power lines can be switched off and through which the above mentioned EFB shutdown signal can be sent to the EFBs.

Level 2 compliance

To claim ARINC 828 level 2 compliance, an aircraft should, in addition to being level 1 compliant, provide:

- Read access to some avionics data to the EFB. Avionics data should be provided in accordance with ARINC Specification 828, Section 3, and ARINC Specification 834.
- WOW (Air/Ground logic) weight on wheels (AC_DISC_1 discrete)
- Aircraft AC/DC Power Available (AC_DISC_2 discrete)

Level 3 compliance

To claim ARINC 828 level 3 compliance, an aircraft should, in addition to being level 2 compliant, provide the space provisions described in Appendix E.

Data compliance

To claim ARINC 828 Data compliance, an aircraft should, in addition to being at least level 1 compliant, provide to the EFB at least all avionics parameters listed in the generic parameter tables included in ARINC Specification 834. The data parameters provided to the EFB should reflect the possibilities of the aircraft type. New generation aircraft with ARINC 828 installation are expected to provide more parameters to the EFB then older legacy aircraft.

Terminal compliance

To claim ARINC 828 Terminal compliance, an aircraft should, in addition to being at least level 1 compliant, provide to the EFBPUs:

- Access to cockpit integrated EFB Terminals via ARINC 828 J2 connectors, or access to side wall mounted EFB Terminals via ARINC 828 (J2 and J4) or (J2 and J5) connectors. Appendix F requirements applies for EFB Terminal installation.
- Video cross linking should be possible and may require the ARINC 828 J3 connectors and the use of the two discretes on J1.

Printing compliance

To claim ARINC 828 Printing compliance, an aircraft should, in addition to being at least level 1 compliant, provide access to an installed ARINC 740/744/744A printer.

Communication compliance

To claim ARINC 828 Communication compliance, an aircraft should, in addition to being at least level 1 compliant, provide bi-directional access to an installed Communication Management Unit (CMU) or Aircraft router, either directly in accordance with ARINC 758 or as described in ARINC 821.

Network Storage compliance

To claim ARINC 828 File Storage compliance, an aircraft should, in addition to being at least level 1 compliant, provide bi-directional access to a Network Storage Device.

1.6 Reference Documents

The following standards and regulatory documents contain provisions which, through reference in this document, constitute provisions of this standard. At the time of publication, the editions if indicated were valid. Because all standards are subject to revision, users of this document are expected to investigate the possibility of applying the most recent edition of these industry standards.

AC 120-76A: *US FAA Advisory Circular Guidelines for Certification, Airworthiness, and operational approval of Electronic Flight Bag Computing Devices*

AC 91.21-1A: *US FAA Advisory Circular Use of Portable Electronic Devices Aboard Aircraft*

AC 20-159: *Obtaining Design and Production Approval of Airport Moving Map Display Applications Intended for Electronic Flight Bag Systems*

AC 25-11-1X Draft: *FAA Advisory Circular Electronic Flight Deck Displays*

ANSI/NEMA WD 6-2002: *Wiring Device – Dimensional Specifications*

ARINC Specification 429: *Mark 33 Digital Information Transfer System*

ARINC Specification 633: *AOC Air-Ground Data and Message Exchange Format*

ARINC Specification 647A: *Flight Recorder Electronic Documentation (FRED)*

ARINC Specification 664 Part 2: *Aircraft Data Network, Ethernet Physical and Data Link Layer Specification*

ARINC Characteristic 702A: *Advanced Flight Management Computer System*

ARINC Characteristic 717: *Flight Acquisition and Recording System*

ARINC Characteristic 758: *Communications Management Unit (CMU)*

ARINC Characteristic 763: *Network Server System (NSS)*

ARINC Characteristic 763A: *Mark 2 Network Server System (NSS) Form and Fit Definition*

ARINC Report 821: *Network Server System (NSS) Functional Definition*

ARINC Specification 834: *Aircraft Data Interface Function (ADIF)*

Digital Visual Interface (DVI) 1.0: *April 2, 1999*

EIA RS-232: *ANSI/TIA/EIA-232-F*

EIA RS-422: *ANSI/TIA/EIA-422-B*

FAA Notice N8200.98: *This Job Aid provides guidance for all Flight Standards District Offices (FSDO), including principal inspectors (PI) that oversee and authorize operators to use EFB computing devices for operational flights in accordance with Title 14 Code of Federal Regulations Parts 91,121, 125, 129 and 135.*

Low Voltage Differential Signaling (LVDS): *ANSI/TIA/EIA-644-A, 2001*

Low Voltage Differential Signaling (LVDS): *IEEE 1596.3-1996*

PL No. 500-017: *Canadian Transport Canada Policy Letter Certification of Electronic Flight Bags (EFBs)*

PS/2: *Personal System/2, IBM 1987*

RFC 6143: *Internet Engineering Task Force (IETF) Request for Comments: 6143, Category: Informational, ISSN: 2070-1721, published March 2011 (also known as the Remote Frame Buffer Protocol).*

TGL 36: JAA Temporary Guidance Leaflet Approval of Electronic Flight Bags (EFBs)

Universal Serial Bus (USB) Revision 2.0: *July 16, 2007*

1.7 RTCA and EUROCAE Documents

RTCA and EUROCAE develop Minimum Operational Performance Standards (MOPS) that are applicable to avionics equipment, systems, and processes. The latest revision of RTCA and EUROCAE documents pertain to this standard, in particular:

RTCA DO-160E/EUROCAE ED-14E – *Environmental Conditions and Test Procedures for Airborne Equipment*

COMMENTARY

The installer may in some circumstances find it necessary or desirable to exceed the minimum environmental levels specified in DO-160E/ED14E. Example environmental tests are identified in Appendix J to this document.

1.8 Regulatory Approval

Implementation of this standard should meet all applicable regulatory requirements.

Manufacturers are urged to obtain all necessary information for such regulatory approval. This information is not contained in this specification, nor is it available from ARINC.

2.0 INTEROPERABILITY STANDARDS

This document specifies standard signal format interface definition to ensure the highest level of interoperability possible. This section defines the electrical signal parameters that must be met to be ARINC 828 compliant. All signals are defined and measured at the associated Reference Plane. This specification pertains to the following types of Physical Layer implementations:

- ARINC 664 Ethernet
- DVI
- LVDS
- USB
- PS/2
- RS-232
- RS-422
- ARINC 429
- ARINC 717
- Discrete

A future Supplement to this standard is expected to define optical signal parameters and physical contacts.

2.1 Reference Plane

The signal reference plane is a performance boundary location that specifies the various Physical Layer implementations transmitter and receiver signals parameters values. The reference plane is located at the ARINC 828 J1 through J7 shipside connector.

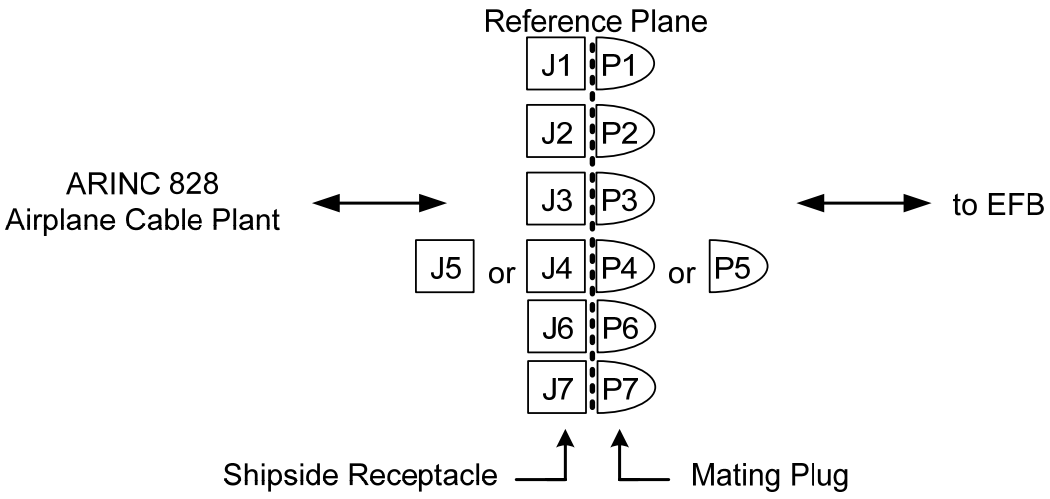

Figure 2-1 – Reference Plane

The electrical wiring interconnects, shielding, and bonding should follow the specific aircraft manufacture practices as defined in their standard practices. In regard to retrofit installations the EFB manufacturer's installation manual, in conjunction with the airframe Standard Practices Manual (typically referred to as Chapter 20), should provide direction for the wiring interconnect requirements.

2.2 Standardized Signaling

EFB electrical signals should be in the form of a digital format or switch contact. The intention of the established standards is to assure the desired interoperability of EFB equipment.

Basic standards described below are applicable to all signals. Unless otherwise specified, signals should conform to the standards set forth in the sections below.

In the sections below the term “input” refers to inputs to EFB and the term “output” refers to outputs from the EFB.

2.2.1 Digital Interfaces

The EFB interface should contain necessary digital interfaces and adequate spares to support growth functions over the foreseeable future.

It is desirable to use the signal types as defined by existing commercial standards, e.g., defined by ANSI, IEEE, etc. If the definition of these signals is insufficiently detailed for use in an aircraft environment, then additional measurements may be needed. Any such measurements should be measured at the signal reference plane.

COMMENTARY

ARINC 828 advocates the specification of a signal reference plane for all high-speed digital signals used in an EFB installation. While this has been available for ARINC 664 Ethernet signals, defined by ARINC 664 Part 2, the EFB Subcommittee recognized that a reference plane needs to be specified for each of the other digital signals. Supplement 1 introduces the signal reference planes for LVDS and USB signals. A future Supplement will include a reference plane for DVI.

2.2.1.1 ARINC 429 Data Bus

ARINC Specification 429 and applicable ARINC Characteristics (e.g., ARINC 702A, ARINC 717) define data word formats, refresh rates, and resolution. The installed wiring should be capable of supporting both low-speed and high-speed operation. See ARINC Specification 429 for additional information.

2.2.1.2 ARINC 664 Ethernet Bus

ARINC Specification 664 defines the physical layer for copper and fiber optic media used in aircraft installations. Exact data word formats, refresh rates, and resolution are to be defined by the airframe manufacturer.

Cable selection, aircraft installation design, and verification should ensure that the performance objectives stated in the above specification are met taking into due consideration the cable distances between the ARINC 828 connector and the Ethernet end points considered.

In this context, demonstration of compliance to eye pattern mask requirements described in ARINC Specification 664, Part 2, is recommended.

2.2.1.3 LVDS

ANSI/TIA/EIA-644-A defines the physical and link layer definitions applicable to Low Voltage Differential Signal (LVDS) signals and data transfers.

Cable selection, aircraft installation design, and verification should ensure that the performance objectives stated in the above specification are met taking into due consideration the cable distances between the ARINC 828 connector and the LVDS end points considered.

In this context, demonstration of compliance to eye pattern mask requirements identified in LVDS specifications is recommended. Appendix G-1 provides illustrations and equations that may be used to calculate the permissible link parameters for any complete LVDS video link as defined from transmitter to receiver. Guidelines are given for division of the complete link into EFB and aircraft allocations. A test case is demonstrated.

2.2.1.4 DVI

Digital Visual Interface (DVI) Version 1.0 defines the physical and link layer definitions applicable to DVI signals and data transfers.

Cable selection, aircraft installation design, and verification should ensure that the performance objectives stated in the above specification are met taking into due consideration the cable distances between the ARINC 828 connector and the DVI end points considered.

In this context, demonstration of compliance to eye pattern mask requirements identified in DVI specifications is recommended.

Appendix G-2 is reserved for the DVI link budget and signal eye pattern. It will be added in a future supplement.

2.2.1.5 USB

Universal Serial Bus (USB) Revision 2.0 defines the physical and link layer definitions applicable to USB signals and data transfers.

Cable selection, aircraft installation design, and verification should ensure that the performance objectives stated in the above specification are met, taking into due consideration the cable distances between the ARINC 828 connector and the USB end points considered.

In this context, demonstration of compliance to eye pattern mask requirements identified in USB specifications is recommended. The link budget and signal eye pattern is defined in Appendix G-3.

2.2.1.5.1 USB Long-Haul

In some EFB installations it is desirable to run USB signals over distances that exceed the 5 meter maximum cable length specified by the USB 2.0 standard. In this case the USB signal may be bridged by means of a repeater or transceiver using a long-haul signaling protocol such as Ethernet bus or high-speed RS422 bus. For the long-haul signaling definition, the link definition must comply with best industry practices for the bridge protocol implemented, taking into consideration any further restrictions imposed by the aircraft environment.

USB Long Haul hardware may be implemented internally to the EFBPU or as an additional external LRU. Definition of the hardware implementation is beyond the scope of this document. Any USB Long-Haul device introduced onto a commercial aircraft as an additional LRU must meet all required qualifications for the installation and the environment.

2.2.1.6 Aircraft Link Tests

2.2.1.6.1 First-of-type Installation Tests

To validate the as-installed condition of the aircraft cabling's ability to support error-free high-speed digital operations, means should be provided to conduct an end-to-end link performance test. The tests should ensure proper signal margins are available to ensure adequate signal performance over the life of the installation. Guidelines for link testing are provided in Appendix G for LVDS, DVI, and USB and in ARINC 664 for Ethernet.

2.2.1.6.2 Line Maintenance Tests

Test criteria for aircraft maintenance and return to service should be provided for line maintenance operations. These tests can be used to assist in the troubleshooting and verification of an installation after repairs or replacements are made.

For line maintenance testing, high-speed digital signals are divided in video signals and data signals.

The preferred way of testing video signals is by presenting a test picture generated by the EFBPU on the EFB Terminal. Interpreting the generated test picture provides information on the health of the video signal. Guidelines for testing video signals are given in Appendix G.

When testing data signals, a typical test involves substituting some or all LRUs at each end of the aircraft cable link with test equipment designed to characterize the cable performance.

2.2.1.7 Printer Interface

As an option, the EFB may use a printer installed at a flight deck location. This may require use of either ARINC 429 or Ethernet interfaces depending on the type of printer installed. Six pins are specified on J3 for use with the printer. See Table 4-3 and Table 4-7 for details.

COMMENTARY

Most aircraft use either a narrow column printer that conforms to ARINC Characteristic 740 or a full-format printer that conforms to ARINC Characteristic 744. Full-format printers with additional graphical capability conform to ARINC Characteristic 744A. A printer with color capability may be used.

2.2.2 Discrete Interfaces

2.2.2.1 Standard Open

The standard "open" signal is characterized by a resistance of 100,000 ohms or more with respect to signal common.

COMMENTARY

In many installations, a single switch is used to supply a logic input to several LRUs. One or more of these LRUs may utilize a pull up resistor in its input circuitry. The result is that an "open" may be accompanied by the presence of 27.5 Vdc nominal. The typical signal range is 18.5 to 36 Vdc.

2.2.2.2 Standard “Ground”

A standard “ground” signal may be generated by either a solid state or mechanical type switch. For mechanical switch type circuits, resistance of 10 ohms or less to signal common represents the “ground” condition. Semiconductor circuitry should exhibit a voltage of 3.5 Vdc or less with respect to signal common in the ground condition.

2.2.2.3 Standard “Applied Voltage” Output

The standard “applied voltage” is defined as having a nominal value of 27.5 Vdc. This voltage is considered “applied” when the actual voltage under the specified load conditions exceeds 18.5 volts (36 Vdc maximum) and is “not applied” when the equivalent impedance to the voltage source exceeds 100,000 ohms.

2.2.2.4 Standard Discrete Input

A standard discrete Input should recognize incoming signals with two possible states “open” and “ground,” where open=1 and ground=0. The characteristics of these two states are defined in Sections 2.2.2.1 and 2.2.2.2 of this document. The maximum current flow in the steady “ground” state should not exceed 20 milliamps.

The “true” state may be represented by either of the two states (ground or open) depending on the aircraft configuration.

The maximum input capacitance to ground should be less than 1 microfarad.

COMMENTARY

The maximum input capacitance is specified because excessive input capacitance can cause current spikes of over 1 amp.

The logic sources for discrete inputs to the EFB are expected to take the form of switches mounted on the airframe component (flap, including gear, etc.) from which the input is desired. These switches can either connect the discrete input pins on the connector to airframe DC ground or leave them open circuit as necessary to reflect the physical condition of the related components.

The EFB is expected to provide the DC signal to be switched. Typically, this is done through a pull-up resistor. The EFB input should sense the voltage on each input to determine the state (open or closed) of each associated switch.

The values of voltages (and resistance) which define the state of an input are based on the assumption that the discrete input utilizes a ground-seeking circuit. The input may utilize an internal pull-up to provide for better noise immunity when a true “open” is present at the input. This type of input circuit is favorable among both manufacturers and users.

Because the probability is quite high that sensors (switches) will provide similar information to a number of users, unwanted signals may be impressed on the EFB inputs, especially when the switches are in the open condition. For this reason, equipment manufacturers should base their logic sensing on the “ground” state of each input. Manufacturers should ensure adequate signal isolation to prevent

sneak circuits from contaminating the logic. Typically diode isolation is used in the avionics equipment to prevent this from happening.

2.2.2.5 Standard Discrete Output

A standard discrete output should exhibit two states, “open” and “ground” as defined in Sections 2.2.2.1 and 2.2.2.2 of this document. In the “open” state, provision should be made to present an output resistance of at least 100,000 ohms. In the “ground” state provision should be made to sink at least 20 milliamps of steady state current. Non-standard current sinking capability may be defined.

COMMENTARY

It is recognized that not all Discrete output needs can be met by the standard discrete output defined above. Some discrete outputs may need to sink more current than the standard value specified above.

The designer is cautioned that discrete input capacitance and discrete output slew rates can caused current spikes of over 1 amp.

Discrete outputs that need to source current should utilize the standard “Applied Voltage” output defined in Section 2.2.2.3. These special cases are noted in the text describing each applicable discrete output function and in the notes to interwiring.

Although defined here, discrete outputs which provide a current output rather than a current sink are not “Standard Discrete Outputs.”

2.2.3 Analog Interfaces

2.2.3.1 DC Panel Backlight Dimming Bus Input

0 to 10 Vdc signal input should be used to control the brightness of the control panel back lighted legends if external brightness control is implemented.

2.2.3.2 AC Panel Backlight Dimming Bus Input

As an alternate to the 10 Vdc Backlight Dimming Bus, 0 to 5 Vac (360-800 Hz) can be used for panel backlighting.

2.3 Power Supply to EFB

The aircraft is expected to provide a minimum of 170 VA to the ARINC 828 connector J1. This power may be 115 Vac (360 to 800 Hz) supply and/or 28 Vdc supply. In either case, the power must be sufficient to supply all appliances on the flight deck side of the ARINC 828 interface. For example, this may include EFBPU, Terminal Device, AID, and so forth.

The EFB installation is expected to meet all applicable EASA and FAA requirements for aircraft power and battery power.

COMMENTARY

The NEMA 5-15R power receptacle installed in cockpits for EFB use should also comply with these electrical requirements.

2.4 EFB Connector Overview

The EFB interface comprises a set of ~~four Mil-Std-38999 type~~ connectors that may be implemented in one of the configurations as shown in Table 2-1 below:

Table 2-1 – EFB Connector Characteristics

Config No.	Conn. Combination	Supports EFBs Mentioned in Use Case	Description/Typical Characteristic of the Connector Combination
1	J1, J2, J3, J4	all	Full set of capabilities.
2	J1, J2, J3	1, 4, 5, 6, 8	This combination supports architectures with OEM installed terminals or EFB platforms that integrate a terminal to the EFBPU.
3	J1, J2	1, 4, 6, 8	This combination supports architectures with OEM installed terminals or EFB platforms that integrate a terminal to the EFBPU. It does not support aftermarket installed displays. The EFBPU interface with the aircraft is limited to the connections defined by J1 and J2.
4	J1, J3, J4/J5	1, 4, 8	This combination limits the EFBPU interface with a physically separated terminal, since it excludes the connections defined by J2, e.g., EFBPU cannot send video signals to a remote terminal. If J5 is used in place of J4 then the limitations of Appendix K apply.
5	J1, J2, J4/J5	1, 4, 6, 8	This combination limits the EFBPU interface with the aircraft, since it excludes the connections defined by J3. If J5 is used in place of J4 then the limitations of Appendix K apply.
6	J1, J3	1, 4, 8	This combination limits the EFBPU interface with a physically separated terminal, since it excludes the connections defined by J2. e.g., EFBPU cannot send video signals to a remote terminal. It does not support the installation of an after-market display.
7	J1, J4/J5	1, 4, 8	An EFBPU can not send video signals to a terminal physically separated from the EFBPU, but it allows the installation of an after market terminal. The EFBPU can only exchange data with the aircraft over a limited number of interfaces. If J5 is used in place of J4 then the limitations of Appendix K apply.
8	J1	1, 4, 8	This combination limits the EFBPU interface with the aircraft to the connections defined by J1. It also limits the installation of a terminal physically separated from the EFBPU and does not support the connection to an after market display.
9	J4/J5	none	This combination supports the connectivity of an EFBPU installed with an after-market installed terminal or display. It is not compliant to ARINC 828.
10	J6, J7, ~~J4~~	all	This combination supports the Ethernet connectivity of an EFBPU interface with the aircraft. ~~Network File Server to the connections defined by J6.~~

2.4.1 Primary ARINC 828 Connector (J1)

ARINC 429 receiver (Primary Avionics Data Source such as FMS)

ARINC 717 receiver (FDR/QAR Data Bus)

Ethernet (2x) for connectivity to Ethernet switch, other EFB, file server, printer, etc.

USB (Primary Device) or as a replacement for an unserviceable Ethernet

Aircraft Discretes – aircraft-specific or platform-specific (WOW, etc.)

EFB discretes - Reset, Device Location, EFB Status, Shutdown Signal, Video Cross-Link

Aircraft power: 28 Vdc and/or 115 Vac

2.4.2 AID to Terminal Connector (J2)

Primary video (LVDS or DVI)

USB ports for display unit control

Aircraft discretes

EFB lighting (aircraft inputs, dimming bus)

Power from AID to display unit

2.4.3 Secondary Avionics and Communications Connector (J3)

ARINC 429 (7x) – Seven connections provisioned (5 reserved for ARINC 429 receivers, two reserved for ARINC 429 (RX or TX))

ARINC 717 (FDR/QAR Data Bus)

Ethernet - Cross EFB connection plus auxiliary interface to display unit

RS-422 Communication

RS-232 - Basic RS-232 TX/RX/GND

RS-232 w/ Flow Control

Video Cross-Link

ARINC 740/744 Printer Interface

2.4.4 AID to Terminal Connector (J4 is similar to J2 with different keying)

Primary video (LVDS or DVI)

USB ports for display unit control

Aircraft discretes

EFB lighting (aircraft inputs, dimming bus)

Power from AID to display unit

2.4.5 AID to Terminal Connector (J5 is an alternative to J4)

Connectors J5-1 and J5-2 are intended as a smaller alternative terminal connector for J4. By removing signals and splitting the remaining signals into two smaller connectors, mechanical installation can be easier. The details are shown in Appendix K.

2.4.6 Fiber Optic Connector (J5)

This connector will use a combination of fiber optic contacts and copper signal contacts.

COMMENTARY

The definition of this connector is under review. At the time of Supplement 2 development, there was no connector definition available. The definition of this connector will be provided in a future Supplement.

2.4.7 Alternate Pin Assignments for the Primary ARINC 828 Connector J1A

This connector assigns an Ethernet signal to the “A” designated Quadrax contact.

2.4.8 Lightweight Ethernet Connector J6

This connector has a single Quadrax contact intended to support 100BaseT Ethernet connection.

2.4.9 Lightweight Power Connector J7

This connector has 5 contacts and is intended to supply either DC or AC power and provide two discretes.

COMMENTARY

The lightweight J6 and J7 connectors are added to support installations of separate EFB Processing Units and display terminals with aircraft networks where only Ethernet and power are needed. Alternate pin assignments for the primary ARINC 828 Connector are defined as J1A.

2.5 Connector Cross-Wiring

2.5.1 Supplement 1 Basic Content

Some EFB installations may require cross-wiring of high-speed digital signals where signal integrity must be preserved. Examples include cross-video signals (J3 to J3), terminal Interconnection (J2 to J4), Ethernet interconnection (J1 to J1).

ARINC Specification 664, Part 2, specifies the wiring techniques and conventions used for wiring Star Quad cable. These techniques are expected to be applied to all Ethernet signals.

COMMENTARY

For non-Ethernet signals (USB, RS422, LVDS, etc.) there are currently no standards available for signal assignment-versus-pin numbers for an LRU that uses a Quadrax contact. This led to the introduction of connectors J3A and J4A specified in APPENDIX H.

2.5.2 Supplement 2 Alternate Pin Requirements

EFB installations that are compliant with ARINC 828-1, which use Star Quad cable for non-Ethernet signals on the J3 and J4 Quadrax contacts may have wiring implementations that do not follow the best practices for terminating Star Quad cable, as defined by ARINC Specification 664 Part 2

Supplement 2 to ARINC 828 creates alternate pin assignments that allow uniformity in wiring Star Quad cables to Quadrax contacts, regardless of the signal type (Ethernet, USB, RS-422, LVDS, DVI, etc.). These alternate pin allocations for connectors J3 and J4, referred to as J3A and J4A respectively, are defined in Appendix H.

The physical connectors, J3A and J4A, are part number identical to the J3 and J4 connectors. Only the pin assignments for the Quadrax contacts that support USB, LVDS and DVI signals have changed.

References to J3 and J4 elsewhere in this document are understood to mean J3A and J4A as well.

Some aircraft manufacturers have indicated that they will only support Supplement 2, Appendix H, alternate pin requirements, as it allows the application of best practices for wiring Star Quad cable as defined in ARINC Specification 664 Part 2.

2.5.3 Supplement 3 RFB Terminal Option – Ethernet Wiring

Appendix L, introduced in Supplement 3, adds an Ethernet interface between the J2 and J4 connectors to support the RFB Terminal option. Quadrax contacts on the J2 and J4 connectors that were previously assigned for LVDS or DVI applications are used for this Ethernet interface. The Ethernet signal assignments for the J2 and J4 quadrax contacts are defined in Appendix L.

Appendix L contains two wiring implementations for the J4 connector. Those installations that use Star Quad cable will use the signal assignment definition identified as “J4A” in Appendix L. This ensures conformance to the best practices for terminating Star Quad wire as defined in ARINC Specification 664, Part 2.

Those aircraft installations that use individual twisted shielded pair wire, as opposed to Star Quad wire, may use the signal assignment definition identified as "J4" in Appendix L. This ensures compatibility with some legacy EFB aircraft installations put in service prior to Supplement 3 standard adoption.

2.5.4 Supplement 4 – Lightweight Connectors

Appendix M, introduced in Supplement 4, adds two new light weight connectors (J6- Ethernet and J7- power). These are added to support installations of separate EFB Processing Units and Display Units in aircraft networks where only Ethernet and power are required. An alternate pin assignments for the primary J1 connector are also defined as J1A.

3.0 AIRCRAFT DATA INTERFACE SERVICES AND PARAMETERS

This document specifies the use of **ARINC Specification 834:** *Aircraft Data Interface Function.* ARINC Specification 834 specifies the avionics interfaces protocols and services to be used by the software applications hosted by the EFB.

3.1 Aircraft Data Interface Services

The aircraft is expected to source data to the EFBPU in a standardized format that is easily read by the EFBPU. The standard EFBPU application interface for aircraft data is defined in ARINC Specification 834, using XML via TCP.

This XML interface could be accomplished in the AID or in the NSU. In either case, the source equipment should provide the appropriate driver for the EFBPU. It is the responsibility of the AID or NSU supplier to provide the XML data translation and the communication protocol services.

3.2 Aircraft Data Parameters

The format of aircraft data parameters is defined in ARINC Specification 834. The parameters are intended for reference only and are not an all inclusive set.

COMMENTARY

The data parameters specified in ARINC Specification 834 are extracted from several existing ARINC Standards including ARINC Specification 429, ARINC Specification 633 and ARINC Characteristic 763. Other aircraft parameters, including those not specified by an ARINC Standard, may be of interest to EFB software applications.

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

This section specifies the common EFB connectors, contacts and signal pin assignments. It represents the collection of signals needed to install EFB equipment on a broad survey of aircraft. The aircraft-wired connectors may be installed at the aircraft sidewall, they may be capped and stowed, or they may be installed in any manner deemed to be good commercial practice.

At the time of this writing, Mil Std references are unavailable for ARINC 828 connectors. European Norm EN3645, defines connectors, electrical, circular, scoop-proof, triple start threaded coupling, with operating temperatures 175 °C or 200 °C continuous. The document has been updated to include the ARINC 828 contact arrangements.

The EN connector references are:

J1: EN3645-F0JL20FA

J1A: EN3645-F0JL20FA

J2: EN3645-F0JL17FA

J3: EN3645-F0JL17FB

J4: EN3645-F0JL17FC

J5-1: EN3645-F0GL75BN

J5-2: EN3646-RS01626BN

J6: EN3645M0AQ01FN

J7: EN3645M0BN05FN (DC Power)

J7: EN3645M0BN05FA (AC Power)

Example connectors follow:

J1: TVP00RQF-25-20SA (i.e., Amphenol part number or equivalent)
J2: TVP00RQF-25-17SA (i.e., Amphenol part number or equivalent)
J3: TVP00RQF-25-17SB (i.e., Amphenol part number or equivalent)
J4: TVP00RQF-25-17SC (i.e., Amphenol part number or equivalent)

OR

J1: 8D0Q25F80SA308L (i.e., Souriau part number or equivalent)
J2: 8D0Q25F87SA308L (i.e., Souriau part number or equivalent)
J3: 8D0Q25F87SB308L (i.e., Souriau part number or equivalent)

COMMENTARY

All “J” connectors are called receptacles and their contacts are sockets. Connector backshells and shell style are not defined in this standard, as they are aircraft installation dependent.

The “P” mating connectors are called plugs and their contacts are pins. They are not defined by this standard.

The EFB connectors and pins specified in this section represent the known and expected interfaces that should be accommodated. This list is not intended to represent a “Required” compliment of aircraft interfaces. It is understood that each

aircraft interface may need to be different to satisfy the EFB connectivity, and therefore, may vary by aircraft type and even by customers of same aircraft type.

Some connector pins are defined as dual function and are identified as such within the following connector tables. Examples of such dual function use are:

1. LVDS and DVI display driver (only one type of display type per aircraft is recommended)
2. Secondary USB and PS/2
3. 10/100BaseT (Ethernet 1 and 4) and 1000BaseT Ethernet (GbE)
4. 10/100BaseT (Ethernet 2) and Video cross-link

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Table 4-1 – J1 Connector Description by Location of Socket

Connector	Location	Abbrev	Description	Type
J1	1	AC_DISC_GND	AC ground can be used for signal guard in pin allocation	#20
J1	2	28VDC	28Vdc Power	#12
J1	3	115VAC	115Vac Power	#12
J1	4	EFB_DISC_GND	EFB ground can be used for signal guard in pin allocation	#20
J1	5	28VDC_RTN	28Vdc_Return Power	#12
J1	6	X_VIDEO_IN	Reserved for mfg assigned video function	#20
J1	7	X_VIDEO_OUT	Reserved for mfg assigned video function	#20
J1	A-1	USB_1_PWR	USB +5V power (0.5A max)	Quadrax
J1	A-2	USB_1_D+	USB Data + {5m max length}	Quadrax
J1	A-3	USB_1_GND	USB Ground return	Quadrax
J1	A-4	USB_1_D-	USB Data - {5m max length}	Quadrax
J1	A-S	USB_1_SH	USB Shield	Quadrax
J1	B	EFB_DISC_2B	Device identification discrete for automatic device configuration J1-B is Bit 1 (MSB) where 0=gnd and 1=open ID / MSB J1-B / LSB J1-Z EFB_1 / 0 / 0 EFB_2 / 0 / 1 EFB_3 / 1 / 0 EFB_4 to n / 1 / 1	#20
J1	C	AC_DISC_1	WOW (Air/Ground logic) weight on wheels	#16
J1	D	AC_DISC_3	Reserved for mfg assigned function	#16
J1	E	A717_1_RX+	ARINC 717 RX Data+	#16
J1	F	A717_1_RX-	ARINC 717 RX Data-	#16
J1	G	AC_DISC_GND	AC ground can be used for signal guard in pin allocation	#20
J1	H-1	10/100 ETH 4_TX+ 1000 BI_DC+	Ethernet Transmit +	Quadrax
J1	H-2	10/100 ETH 4_RX+ 1000 BI_DD+	Ethernet Receive +	Quadrax
J1	H-3	10/100 ETH 4_TX- 1000 BI_DC-	Ethernet Transmit -	Quadrax
J1	H-4	10/100 ETH 4_RX- 1000 BI_DD-	Ethernet Receive -	Quadrax
J1	H-S	ETH 4_SH	Ethernet Shield	Quadrax
J1	J	Chassis	Chassis Safety Ground	#16
J1	K-1	10/100 ETH 1_TX+ 1000 BI_DA+	Ethernet Transmit +	Quadrax
J1	K-2	10/100 ETH 1_RX+ 1000 BI_DB+	Ethernet Receive +	Quadrax
J1	K-3	10/100 ETH 1_TX- 1000 BI_DA-	Ethernet Transmit -	Quadrax
J1	K-4	10/100 ETH 1_RX- 1000 BI_DB-	Ethernet Receive -	Quadrax
J1	K-S	ETH 1_SH	Ethernet Shield	Quadrax
J1	L	EFB_DISC_GND	EFB ground can be used for signal guard in pin allocation	#20

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J1	M	EFB_DISC_3	Shutdown signal (On/Off)	#16
J1	N	A429_1_RX-	ARINC 429 Receiver -	#16
J1	P	A429_1_RX+	ARINC 429 Receiver +	#16
J1	R	EFB_DISC_1	Reset	#16
J1	S	EFB_DISC_5	Unit gets power from aircraft.	#20
J1	T	AC_DISC_2	Aircraft AC/DC Power Available (to know if a certain bus is powered)	#16
J1	U	AC_DISC_4	Reserved for mfg assigned function	#16
J1	V	A717_1_RXSH	ARINC 717 RX Shield	#20
J1	W	115VAC_RTN	115Vac Return Power	#12
J1	X	EFB_DISC_4	Unit active	#20
J1	Y	A429_1_RXSH	ARINC 429 RX Shield	#16
J1	Z	EFB_DISC_2A	Device identification discrete for automatic device configuration J1-Z is Bit 0 (LSB) where 0=gnd and 1=open	#16

ID	MSB J1-B	LSB J1-Z
EFB_1	0	0
EFB_2	0	1
EFB_3	1	0
EFB_4 to n	1	1

Table 4-2 – J2 Connector Description by Location of Socket

Connector	Location	Abbrev	Description	Type
J2	a	DispDCPWR	Power from AID to display	22D
J2	A-1	FP_D0+	LCD flat panel data line 0 (R2-7,G2)	Quadrax
		TMDS_D0+	DVI Data Line 0. Note: only single link	
J2	A-2	FP_D1+	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
		TMDS_CLK+	DVI Clock	
J2	A-3	FP_D0-	LCD flat panel data line 0 (R2-7,G2)	Quadrax
		TMDS_D0-	DVI Data Line 0	
J2	A-4	FP_D1-	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
		TMDS_CLK-	DVI Clock	
J2	A-S	AS_SH	Shield	Quadrax
J2	B	Ground	Ground	22D
J2	b	AC_DISC_5	Reserved for aircraft specific discrete	22D
J2	C	Ground	Ground	22D
J2	c	Ground	Ground	22D
J2	d	AC_DISC_6	Reserved for aircraft specific discrete	22D
J2	D-1	FP_D2+	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
		TMDS_D1+	DVI Data Line 1	
J2	D-2	FP_D3+	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
		TMDS_D2+	DVI Data Line 2	
J2	D-3	FP_D2-	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
		TMDS_D1-	DVI Data Line 1	
J2	D-4	FP_D3-	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
		TMDS_D2-	DVI Data Line 2	
J2	D-S	DS_SH	Shield	Quadrax
J2	e	28Vdc_ANNUN+	28Vdc Annunciator bus	22D
J2	E	DispDCRtn	Power from AID to display	22D
J2	f	28Vdc_ANNUN-	28Vdc Annunciator bus	22D
J2	F	DispDCRtn	Power from AID to display	22D
J2	g	DISP_3	Reserved for display use	22D
J2	G-1	FP_CLK+	LCD flat panel clock	Quadrax
		DDCCLK	DVI Display Bus Clock	
J2	G-2	FP_D4+	Future LCD flat panel data 4	Quadrax
J2	G-3	FP_CLK-	LCD flat panel clock	Quadrax
		DDCDATA	DVI Display Bus Data	
J2	G-4	FP_D4-	Future LCD flat panel data 4	Quadrax
J2	G-S	GS_SH	Shield	Quadrax
J2	H	Ground	Ground	22D
J2	h	DISP_6	Reserved for display use	22D
J2	J	Ground	Ground	22D
J2	k	DISP_5	Reserved for display use	22D
J2	K-1	USB_2_PWR	USB +5V Power (0.5A max)	Quadrax
		PS2_2_PWR	PS2 Device Power	
J2	K-2	USB_2_D+	USB Data + {5m max length}	Quadrax
		PS2_2_GND	PS2 Device Ground	

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J2	K-3	USB_2_GND	USB Ground return	Quadrax
		PS2_2_CLK	PS2 Device Clock	
J2	K-4	USB_2_D-	USB Data - {5m max length}	Quadrax
		PS2_2_DATA	PS2 Device Data	
J2	K-S	KS_SH	Shield	Quadrax
J2	L	Ground	Ground	22D
J2	M	Ground	Ground	22D
J2	m	DISP_4	Reserved for display use	22D
J2	n	AC_DISC_11	Reserved for aircraft use	22D
J2	N-1	USB_3_PWR	USB +5V power (0.5A max)	Quadrax
		PS2_3_PWR	PS2 Device Power	
J2	N-2	USB_3_D+	USB Data + {5m max length}	Quadrax
		PS2_3_GND	PS2 Device Ground	
J2	N-3	USB_3_GND	USB Ground return	Quadrax
		PS2_3_CLK	PS2 Device Clock	
J2	N-4	USB_3_D-	USB Data - {5m max length}	Quadrax
		PS2_3_DATA	PS2 Device Data	
J2	N-S	NS_SH	Shield	Quadrax
J2	P	Ground	Ground	22D
J2	p	AC_DISC_9	Reserved for aircraft use	22D
J2	q	AC_DISC_7	Reserved for aircraft specific discrete	22D
J2	R	Ground	Ground	22D
J2	r	AC_DISC_8	Reserved for aircraft use	22D
J2	s	5Vac_ANNUN+	5Vac Annunciator bus	22D
J2	S-1	USB_4_PWR	USB +5V power (0.5A max)	Quadrax
		PS2_4_PWR	PS2 Device Power	
J2	S-2	USB_4_D+	USB Data + {5m max length}	Quadrax
		PS2_4_GND	PS2 Device Ground	
J2	S-3	USB_4_GND	USB Ground return	Quadrax
		PS2_4_CLK	PS2 Device Clock	
J2	S-4	USB_4_D-	USB Data - {5m max length}	Quadrax
		PS2_4_DATA	PS2 Device Data	
J2	S-S	SS_SH	Shield	Quadrax
J2	t	5Vac_ANNUN-	5Vac Annunciator bus	22D
J2	T	DispDCPWR	Power from AID to display	22D
J2	U	DispDCPWR	Power from AID to display	22D
J2	u	DISP_2	Reserved for display use	22D
J2	V	Ground	Ground	22D
J2	v	DISP_1	Reserved for display use	22D
J2	W	DispDCRtn	Power from AID to display	22D
J2	w	AC_DISC_10	Reserved for aircraft use	22D
J2	X	DISP_8	Reserved for display use	22D
J2	Y	DISP_7	Reserved for display use	22D
J2	Z	Ground	Ground	22D

Table 4-3 – J3 Connector Description by Location of Socket

Connector	Location	Abbrev	Description	Type
J3	a	RS232_2_GND	RS-232 Return	22D
J3	A-1	ETH 3_TX+	Ethernet Transmit +	Quadrax
J3	A-2	ETH 3_RX+	Ethernet Receive +	Quadrax
J3	A-3	ETH 3_TX-	Ethernet Transmit -	Quadrax
J3	A-4	ETH 3_RX-	Ethernet Receive -	Quadrax
J3	A-S	ETH 3_SH	Ethernet Shield	Quadrax
J3	b	A717_2_RX+	ARINC 717 RX Data+	22D
J3	B	A429_5_RX+	Printer to EFB (Receive +)	22D
J3	C	A429_5_RX-	Printer to EFB (Receive -)	22D
J3	c	A429_4_RXSH	ARINC 429 RX Shield	22D
J3	d	A429_4_RX+	ARINC 429 Receiver +	22D
J3	D-1	X_FP_D0+_TX	Cross LCD Flat Panel Data line 0 (R2-7,G2) TX	Quadrax
		X_TDMS_D0+_TX	Cross DVI Data Line 0_TX	
J3	D-2	X_FP_D1+_TX	Cross LCD Flat Panel Data line 1 (G3-7,B2-3) TX	Quadrax
		X_TDMS_D1+_TX	Cross DVI Data Line 1_TX	
J3	D-3	X_FP_D0-_TX	Cross LCD Flat Panel Data line 0 (R2-7,G2) TX	Quadrax
		X_TDMS_D0-_TX	Cross DVI Data Line 0_TX	
J3	D-4	X_FP_D1-_TX	Cross LCD Flat Panel Data line 1 (G3-7,B2-3) TX	Quadrax
		X_TDMS_D1-_TX	Cross DVI Data Line 1_TX	
J3	D-S	X_D1_SH	Shield	Quadrax
J3	e	A429_3_RX+	ARINC 429 Receiver +	22D
J3	E	A429_2_RX+	ARINC 429 Receiver +	22D
J3	F	A429_2_RX-	ARINC 429 Receiver -	22D
J3	f	A429_3_RX-	ARINC 429 Receiver -	22D
J3	g	RS232_1_CTS	Clear To Send	22D
J3	G-1	X_FP_D2+_TX	Cross LCD Flat Panel Data line 2 (B4-7,HSYNC,VSYNC,DE) TX	Quadrax
		X_TDMS_D2+_TX	Cross DVI Data Line 2_TX	
J3	G-2	X_FP_CLK+_TX	Cross LCD Flat Panel Clock TX	Quadrax
		X_TDMS_CLK+_TX	Cross DVI Clock_TX	
J3	G-3	X_FP_D2-_TX	Cross LCD Flat Panel Data line 2 (B4-7,HSYNC,VSYNC,DE) TX	Quadrax
		X_TDMS_D2-_TX	Cross DVI Data Line 2_TX	
J3	G-4	X_FP_CLK-_TX	Cross LCD Flat Panel Clock TX	Quadrax
		X_TDMS_CLK-_TX	Cross DVI Clock_TX	
J3	G-S	X_D2_SH	Shield	Quadrax
J3	h	RS232_1_DTR	Data Terminal Ready	22D
J3	H	A429_6_TX-	EFB to Printer (Transmitter -)	22D
J3	J	A429_6_TX+	EFB to Printer (Transmitter +)	22D
J3	k	RS232_1_DSR	Data Set Ready	22D
J3	K-1	ETH 2_TX+	Ethernet Transmit +	Quadrax
		X_FP_D0+_RX	Cross LCD Flat Panel Data line 0 (R2-7,G2) RX	
		X_TDMS_D0+_RX	Cross DVI Data Line 0_RX	
J3	K-2	ETH 2_RX+	Ethernet Receive +	Quadrax
		X_FP_D1+_RX	Cross LCD Flat Panel Data line 1 (G3-7,B2-3) RX	
		X_TDMS_D1+_RX	Cross DVI Data Line 1 RX	

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J3	K-3	ETH 2_TX-	Ethernet Transmit -	Quadrax
		X_FP_D0-_RX	Cross LCD Flat Panel Data line 0 (R2-7,G2) RX	
		X_TDMS_D0-_RX	Cross DVI Data Line 0 RX	
J3	K-4	ETH 2_RX-	Ethernet Receive -	Quadrax
		X_FP_D1-_RX	Cross LCD Flat Panel Data line 1 (G3-7,B2-3) RX	
		X_TDMS_D1-_RX	Cross DVI Data Line 1_RX	
J3	K-S	ETH 2_SH	Ethernet Shield	Quadrax
J3	L	A429_7_RTX-	ARINC 429 Receiver or Transmitter -	22D
J3	M	A429_7_RTX+	ARINC 429 Receiver or Transmitter +	22D
J3	m	RS232_1_DCD	Data Carrier Detect	22D
J3	n	RS232_1_GND	RS-232 Return	22D
J3	N-1	X_FP_D2+_RX	Cross LCD Flat Panel Data line 2 (B4-7,HSYNC,VSYNC,DE) RX	Quadrax
		X_TDMS_D2+_RX	Cross DVI Data Line 2_RX	
J3	N-2	X_FP_CLK+_RX	Cross LCD Flat Panel Clock RX	Quadrax
		X_TDMS_CLK+_RX	Cross DVI Clock_RX	
J3	N-3	X_FP_D2-RX	Cross LCD Flat Panel Data line 2 (B4-7,HSYNC,VSYNC,DE) RX	Quadrax
		X_TDMS_D2-_RX	Cross DVI Data Line 2_RX	
J3	N-4	X_FP_CLK-_RX	Cross LCD Flat Panel Clock RX	Quadrax
		X_TDMS_CLK-_RX	Cross DVI Clock_RX	
J3	N-S	X_NS_SH	Shield	Quadrax
J3	p	RS232_1_TX	Transmit Data	22D
J3	P	A429_8_RX-	ARINC 429 Receiver -	22D
J3	q	A717_2_RXSH	ARINC 717 RX Shield	22D
J3	r	A717_2_RX-	ARINC 717 RX Data-	22D
J3	R	A429_8_RX+	ARINC 429 Receiver +	22D
J3	s	A429_4_RX-	ARINC 429 Receiver -	22D
J3	S-1	RS422_TXD+	Transmit Data +	Quadrax
J3	S-2	RS422_RXD+	Receive Data +	Quadrax
J3	S-3	RS422_TXD-	Transmit Data -	Quadrax
J3	S-4	RS422_RXD-	Receive Data -	Quadrax
J3	S-S	RS422_SH	RS422 Shield	Quadrax
J3	t	A429_3_RXSH	ARINC 429 RX Shield	22D
J3	T	RS232_2_TX	Transmit Data	22D
J3	u	RS232_1_RI	Ring Indicator	22D
J3	U	RS232_2_RX	Receive Data	22D
J3	V	A429_5_RXSH	Printer to EFB (RX Shield)	22D
J3	v	RS232_1_RTS	Ready To Send	22D
J3	w	RS232_1_RX	Receive Data	22D
J3	W	A429_2_RXSH	ARINC 429 RX Shield	22D
J3	X	A429_6_TXSH	EFB to Printer (TX Shield)	22D
J3	Y	A429_7_RTXSH	ARINC 429 RX/TX Shield	22D
J3	Z	A429_8_RXSH	ARINC 429 RX Shield	22D

Table 4-4 – J4 Connector Description by Location of Socket

Connector	Location	Abbrev	Description	Type
J4	a	DispDCPWR	Power from AID to display	22D
J4	A-1	FP_D0+	LCD flat panel data line 0 (R2-7,G2)	Quadrax
		TMDS_D0+	DVI Data Line 0 NOTE: only single link supported	
J4	A-2	FP_D1+	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
		TMDS_CLK+	DVI Clock	
J4	A-3	FP_D0-	LCD flat panel data line 0 (R2-7,G2)	Quadrax
		TMDS_D0-	DVI Data Line 0	
J4	A-4	FP_D1-	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
		TMDS_CLK-	DVI Clock	
J4	A-S	AS_SH	Shield	Quadrax
J4	B	Ground	Ground	22D
J4	b	AC_DISC_5	Reserved for aircraft specific discrete	22D
J4	C	Ground	Ground	22D
J4	c	Ground	Ground	22D
J4	d	AC_DISC_6	Reserved for aircraft specific discrete	22D
J4	D-1	FP_D2+	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
		TMDS_D1+	DVI Data Line 1	
J4	D-2	FP_D3+	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
		TMDS_D2+	DVI Data Line 2	
J4	D-3	FP_D2-	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
		TMDS_D1-	DVI Data Line 1	
J4	D-4	FP_D3-	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
		TMDS_D2-	DVI Data Line 2	
J4	D-S	DS_SH	Shield	Quadrax
J4	e	28Vdc_ANNUN+	28Vdc Annunciator bus	22D
J4	E	DispDCRtn	Power from AID to display	22D
J4	f	28Vdc_ANNUN-	28Vdc Annunciator bus	22D
J4	F	DispDCRtn	Power from AID to display	22D
J4	g	DISP_3	Reserved for display use	22D
J4	G-1	FP_CLK+	LCD flat panel clock	Quadrax
		DDCCLK	DVI Display Bus Clock	
J4	G-2	FP_D4+	Future LCD flat panel data 4	Quadrax
J4	G-3	FP_CLK-	LCD flat panel clock	Quadrax
		DDCDATA	DVI Display Bus Data	
J4	G-4	FP_D4-	Future LCD flat panel data 4	Quadrax
J4	G-S	GS_SH	Shield	Quadrax
J4	H	Ground	Ground	22D
J4	h	DISP_6	Reserved for display use	22D
J4	J	Ground	Ground	22D
J4	k	DISP_5	Reserved for display use	22D
J4	K-1	USB_2_PWR	USB +5V power (0.5A max)	Quadrax
		PS2_2_PWR	PS2 Device Power	
J4	K-2	USB_2_D+	USB Data + {5m max length}	Quadrax

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
		PS2_2_GND	PS2 Device Ground	
J4	K-3	USB_2_GND	USB Ground return	Quadrax
		PS2_2_CLK	PS2 Device Clock	
J4	K-4	USB_2_D-	USB Data - {5m max length}	Quadrax
		PS2_2_DATA	PS2 Device Data	Quadrax
J4	K-S	KS_SH	Shield	Quadrax
J4	L	Ground	Ground	22D
J4	M	Ground	Ground	22D
J4	m	DISP_4	Reserved for display use	22D
J4	n	AC_1	Reserved for aircraft specific use	22D
J4	N-1	USB_3_PWR	USB +5V power (0.5A max)	Quadrax
		PS2_3_PWR	PS2 Device Power	
J4	N-2	USB_3_D+	USB Data + {5m max length}	Quadrax
		PS2_3_GND	PS2 Device Ground	
J4	N-3	USB_3_GND	USB Ground return	Quadrax
		PS2_3_CLK	PS2 Device Clock	
J4	N-4	USB_3_D-	USB Data - {5m max length}	Quadrax
		PS2_3_DATA	PS2 Device Data	
J4	N-S	NS_SH	Shield	Quadrax
J4	P	Ground	Ground	22D
J4	p	AC_1	Reserved for aircraft specific use	22D
J4	q	AC_DISC_7	Reserved for aircraft specific discrete	22D
J4	R	Ground	Ground	22D
J4	r	AC_1	Reserved for aircraft specific use	22D
J4	s	5Vac_ANNUN+	5Vac Annunciator bus	22D
J4	S-1	USB_4_PWR	USB +5V power (0.5A max)	Quadrax
		PS2_4_PWR	PS2 Device Power	
J4	S-2	USB_4_D+	USB Data + {5m max length}	Quadrax
		PS2_4_GND	PS2 Device Ground	
J4	S-3	USB_4_GND	USB Ground return	Quadrax
		PS2_4_CLK	PS2 Device Clock	
J4	S-4	USB_4_D-	USB Data - {5m max length}	Quadrax
		PS2_4_DATA	PS2 Device Data	
J4	S-S	SS_SH	Shield	Quadrax
J4	t	5Vac_ANNUN-	5Vac Annunciator bus	22D
J4	T	DispDCPWR	Power from AID to display	22D
J4	U	DispDCPWR	Power from AID to display	22D
J4	u	DISP_2	Reserved for display use	22D
J4	V	Ground	Ground	22D
J4	v	DISP_1	Reserved for display use	22D
J4	W	DispDCRtn	Power from AID to display	22D
J4	w	AC_1	Reserved for aircraft specific use	22D
J4	X	DISP_8	Reserved for display use	22D
J4	Y	DISP_7	Reserved for display use	22D
J4	Z	Ground	Ground	22D

Table 4-5 – J1 Connector Description by Signal Function

Connector	Location	Abbrev	Description	Type
J1		A429_1	Most important avionics data	
J1	P	A429_1_RX+	ARINC 429 Receiver +	#16
J1	N	A429_1_RX-	ARINC 429 Receiver -	#16
J1	Y	A429_1_RXSH	ARINC 429 RX Shield	#16
J1		ARINC 717	ARINC 717 FDR/QAR Data Bus	
J1	E	A717_1_RX+	ARINC 717 RX Data+	#16
J1	F	A717_1_RX-	ARINC 717 RX Data-	#16
J1	V	A717_1_RXSH	ARINC 717 RX Shield	#20
J1	K	Ethernet #1 10/100/1000	Connected to aircraft installed switch or router	
J1	K-1	10/100 ETH 1_TX+ 1000 BI_DA+	Ethernet Transmit +	Quadrax
J1	K-3	10/100 ETH 1_TX- 1000 BI_DA-	Ethernet Transmit -	Quadrax
J1	K-2	10/100 ETH 1_RX+ 1000 BI_DB+	Ethernet Receive +	Quadrax
J1	K-4	10/100 ETH 1_RX- 1000 BI_DB-	Ethernet Receive -	Quadrax
J1	K-S	ETH 1_SH	Ethernet Shield	Quadrax
J1	H	Ethernet #4 10/100/1000	Connection intended for EFB-EFB Cross Over Functionality	
J1	H-1	10/100 ETH 4_TX+ 1000 BI_DC+	Ethernet Transmit +	Quadrax
J1	H-3	10/100 ETH 4_TX- 1000 BI_DC-	Ethernet Transmit -	Quadrax
J1	H-2	10/100 ETH 4_RX+ 1000 BI_DD+	Ethernet Receive +	Quadrax
J1	H-4	10/100 ETH 4_RX- 1000 BI_DD-	Ethernet Receive -	Quadrax
J1	H-S	ETH 4_SH	Ethernet Shield	Quadrax
J1		USB_1	Most important USB device	
J1	A-1	USB_1_PWR	USB +5V power (0.5A max)	Quadrax
J1	A-2	USB_1_D+	USB Data + {5m max length}	Quadrax
J1	A-4	USB_1_D-	USB Data - {5m max length}	Quadrax
J1	A-3	USB_1_GND	USB Ground return	Quadrax
J1	A-S	USB_1_SH	USB Shield	Quadrax
J1		ACDisc1	WOW (Air/Ground logic) weight on wheels	
J1	C	AC_DISC_1	WOW (Air/Ground logic) weight on wheels	#16
J1		ACDisc2	Aircraft AC/DC Power Available (to know if a certain bus is powered)	
J1	T	AC_DISC_2	Aircraft AC/DC Power Available (to know if a certain bus is powered)	#16
J1		ACDisc3	Reserved for aircraft specific discrete	
J1	D	AC_DISC_3	Reserved for mfg assigned function	#16
J1		ACDisc4	Reserved for aircraft specific discrete	
J1	U	AC_DISC_4	Reserved for mfg assigned function	#16
J1		ACDisc Ground	Reserved for aircraft specific discrete	
J1	1	AC_DISC_GND	AC ground can be used for signal guard in pin allocation	#20

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J1	G	AC_DISC_GND	AC ground can be used for signal guard in pin allocation	#20
J1		EFB_Disc_1	Reset	
J1	R	EFB_Disc_1	Reset	#16
J1		EFBDisc2	Device identification discrete for automatic device configuration J1-B is Bit 1 (MSB) ID / MSB J1-B / LSB J1-Z CAPT / 0 / 0 FO / 0 / 1 EFB_3 / 1 / 0 EFB_4 to n / 1 / 1	
J1	Z	EFB_DISC_2A	Device identification discrete for automatic device configuration J1-Z is Bit 0 (LSB)	#16
J1	B	EFB_DISC_2B	Device identification discrete for automatic device configuration J1-B is Bit 1 (MSB)	#20
J1		EFBDisc3	Shutdown signal (On/Off)	
J1	M	EFB_DISC_3	Shutdown signal (On/Off)	#16
J1		EFBDisc4	Unit active	
J1	X	EFB_DISC_4	Unit active	#20
J1		EFBDisc5	Unit gets power from aircraft	
J1	S	EFB_DISC_5	Unit gets power from aircraft	#20
J1		EFBDisc Ground	Unit gets power from aircraft	
J1	4	EFB_DISC_GND	EFB ground can be used for signal guard in pin allocation	#20
J1	L	EFB_DISC_GND	EFB ground can be used for signal guard in pin allocation	#20
J1		AC Power	115Vac Power	
J1	3	115VAC	115Vac Power	#12
J1	W	115VAC_RTN	115Vac Return Power	#12
J1	J	Chassis	Chassis Safety Ground	#16
J1		DC Power	28Vdc Power	
J1	2	28VDC	28Vdc Power	#12
J1	5	28VDC_RTN	28Vdc_Return Power	#12
J1		X_Video	Cross video discretes	
J1	6	X_VIDEO_IN	reserved for mfg assigned video function	#20
J1	7	X_VIDEO_OUT	reserved for mfg assigned video function	#20

Table 4-6 – J2 Connector Description by Signal Function

Connector	Location	Abbrev	Description	Type
J2		Video	DVI or LVDS = 5 twisted pairs = 10 wires	
J2	A-1	FP_D0+	LCD flat panel data line 0 (R2-7,G2)	Quadrax
J2	A-3	FP_D0-	LCD flat panel data line 0 (R2-7,G2)	Quadrax
J2	A-2	FP_D1+	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
J2	A-4	FP_D1-	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
J2	A-S	FP_D1_SH	Shield	Quadrax
J2	D-1	FP_D2+	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
J2	D-3	FP_D2-	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
J2	D-2	FP_D3+	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
J2	D-4	FP_D3-	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
J2	D-S	FP_D2_SH	Shield	Quadrax
J2	G-1	FP_CLK+	LCD flat panel clock	Quadrax
J2	G-3	FP_CLK-	LCD flat panel clock	Quadrax
J2	G-2	FP_D4+	Future LCD flat panel data 4	Quadrax
J2	G-4	FP_D4-	Future LCD flat panel data 4	Quadrax
J2	G-S	FP_D4_SH	Shield	Quadrax
J2	A-1	TMDS_D0+	DVI Data Line 0 NOTE: only single link supported	Quadrax
J2	A-3	TMDS_D0-	DVI Data Line 0	Quadrax
J2	D-1	TMDS_D1+	DVI Data Line 1	Quadrax
J2	D-3	TMDS_D1-	DVI Data Line 1	Quadrax
J2	D-2	TMDS_D2+	DVI Data Line 2	Quadrax
J2	D-4	TMDS_D2-	DVI Data Line 2	Quadrax
J2	D-S	TMDS_DATA_SH	Shield	Quadrax
J2	A-2	TMDS_CLK+	DVI Clock	Quadrax
J2	A-4	TMDS_CLK-	DVI Clock	Quadrax
J2	A-S	TDMS_CLK_SH	Shield	Quadrax
J2	G-1	DDCCLK	DVI Display Bus Clock	Quadrax
J2	G-3	DDCDATA	DVI Display Bus Data	Quadrax
J2		USB_2	Secondary USB device or PS/2	
J2	K-1	USB_2_PWR	USB +5V power (0.5A max)	Quadrax
J2	K-2	USB_2_D+	USB Data + {5m max length}	Quadrax
J2	K-4	USB_2_D-	USB Data - {5m max length}	Quadrax
J2	K-3	USB_2_GND	USB Ground return	Quadrax
J2	K-S	USB_2_SH	USB Shield	Quadrax
J2	K-3	PS2_2_CLK	PS2 Device Clock	Quadrax
J2	K-4	PS2_2_DATA	PS2 Device Data	Quadrax
J2	K-1	PS2_2_PWR	PS2 Device Power	Quadrax
J2	K-2	PS2_2_GND	PS2 Device Ground	Quadrax
J2	K-S	PS2_2_SH	PS2 Shield	Quadrax
J2		USB_3	Secondary USB device or PS/2	
J2	N-1	USB_3_PWR	USB +5V power (0.5A max)	Quadrax

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J2	N-2	USB_3_D+	USB Data + {5m max length}	Quadrax
J2	N-4	USB_3_D-	USB Data - {5m max length}	Quadrax
J2	N-3	USB_3_GND	USB Ground return	Quadrax
J2	N-S	USB_3_SH	USB Shield	Quadrax
J2	N-3	PS2_3_CLK	PS2 Device Clock	Quadrax
J2	N-4	PS2_3_DATA	PS2 Device Data	Quadrax
J2	N-1	PS2_3_PWR	PS2 Device Power	Quadrax
J2	N-2	PS2_3_GND	PS2 Device Ground	Quadrax
J2	N-S	PS2_3_SH	PS2 Shield	Quadrax
J2		USB_4	Secondary USB device or PS/2	
J2	S-1	USB_4_PWR	USB +5V Power (0.5A max)	Quadrax
J2	S-2	USB_4_D+	USB Data + {5m max length}	Quadrax
J2	S-4	USB_4_D-	USB Data - {5m max length}	Quadrax
J2	S-3	USB_4_GND	USB Ground return	Quadrax
J2	S-S	USB_4_SH	USB Shield	Quadrax
J2	S-3	PS2_4_CLK	PS2 Device Clock	Quadrax
J2	S-4	PS2_4_DATA	PS2 Device Data	Quadrax
J2	S-1	PS2_4_PWR	PS2 Device Power	Quadrax
J2	S-2	PS2_4_GND	PS2 Device Ground	Quadrax
J2	S-S	PS2_4_SH	PS2 Shield	Quadrax
J2		Reserved	Reserved for aircraft specific discrete	
J2	b	AC_DISC_5	Reserved for aircraft specific discrete	22D
J2	d	AC_DISC_6	Reserved for aircraft specific discrete	22D
J2	q	AC_DISC_7	Reserved for aircraft specific discrete	22D
J2		Reserved	Reserved for aircraft use	
J2	r	AC_DISC_8	Reserved for aircraft use	22D
J2	p	AC_DISC_9	Reserved for aircraft use	22D
J2	w	AC_DISC_10	Reserved for aircraft use	22D
J2	n	AC_DISC_11	Reserved for aircraft use	22D
J2		EFBLighting	Display lighting, bezel keys lighting, dimming	
J2	e	28Vdc_ANNUN+	28Vdc Annunciator bus	22D
J2	f	28Vdc_ANNUN-	28Vdc Annunciator bus	22D
J2	s	5Vac_ANNUN+	5Vac Annunciator bus	22D
J2	t	5Vac_ANNUN-	5Vac Annunciator bus	22D
J2		DC Power Return	Power from AID to display	
J2	U	DispDCPWR	Power from AID to display	22D
J2	T	DispDCPWR	Power from AID to display	22D
J2	a	DispDCPWR	Power from AID to display	22D
J2	W	DispDCRtn	Power from AID to display	22D
J2	E	DispDCRtn	Power from AID to display	22D
J2	F	DispDCRtn	Power from AID to display	22D
J2		Ground pins	Ground pins	
J2	B	Ground	Ground	22D
J2	V	Ground	Ground	22D
J2	C	Ground	Ground	22D
J2	J	Ground	Ground	22D
J2	H	Ground	Ground	22D

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J2	M	Ground	Ground	22D
J2	L	Ground	Ground	22D
J2	c	Ground	Ground	22D
J2	P	Ground	Ground	22D
J2	R	Ground	Ground	22D
J2	Z	Ground	Ground	22D
J2		Reserved	Reserved for display use	
J2	v	DISP_1	Reserved for display use	22D
J2	u	DISP_2	Reserved for display use	22D
J2	g	DISP_3	Reserved for display use	22D
J2	m	DISP_4	Reserved for display use	22D
J2	k	DISP_5	Reserved for display use	22D
J2	h	DISP_6	Reserved for display use	22D
J2	Y	DISP_7	Reserved for display use	22D
J2	X	DISP_8	Reserved for display use	22D

Table 4-7 – J3 Connector Description by Signal Function

Connector	Location	Abbrev	Description	Type
J3		A429_2	Secondary avionics data	
J3	E	A429_2_RX+	ARINC 429 Receiver +	22D
J3	F	A429_2_RX-	ARINC 429 Receiver -	22D
J3	W	A429_2_RXSH	ARINC 429 RX Shield	22D
J3		A429_3	Secondary avionics data	
J3	e	A429_3_RX+	ARINC 429 Receiver +	22D
J3	f	A429_3_RX-	ARINC 429 Receiver -	22D
J3	t	A429_3_RXSH	ARINC 429 RX Shield	22D
J3		A429_4	Secondary avionics data	
J3	d	A429_4_RX+	ARINC 429 Receiver +	22D
J3	s	A429_4_RX-	ARINC 429 Receiver -	22D
J3	c	A429_4_RXSH	ARINC 429 RX Shield	22D
J3		A429_5	Printer to EFB	
J3	B	A429_5_RX+	Printer to EFB (Receiver +)	22D
J3	C	A429_5_RX-	Printer to EFB (Receiver -)	22D
J3	V	A429_5_RXSH	Printer to EFB (RX Shield)	22D
J3		A429_6	EFB to Printer	
J3	J	A429_6_TX+	EFB to Printer (Transmitter +)	22D
J3	H	A429_6_TX-	EFB to Printer (Transmitter -)	22D
J3	X	A429_6_TXSH	EFB to Printer (TX Shield)	22D
J3		A429_7	Custom	
J3	M	A429_7_RTX+	ARINC 429 Receiver or Transmitter +	22D
J3	L	A429_7_RTX-	ARINC 429 Receiver or Transmitter -	22D
J3	Y	A429_7_RTXSH	ARINC 429 RX/TX Shield	22D
J3		A429_8	Custom	
J3	R	A429_8_RX+	ARINC 429 Receiver +	22D
J3	P	A429_8_RX-	ARINC 429 Receiver -	22D
J3	Z	A429_8_RXSH	ARINC 429 RX Shield	22D
J3		ARINC 717	ARINC 717 FDR/QAR Data Bus	
J3	b	A717_2_RX+	ARINC 717 RX Data+	22D
J3	r	A717_2_RX-	ARINC 717 RX Data-	22D
J3	q	A717_2_RXSH	ARINC 717 RX Shield	22D
J3		Ethernet #2	Directly connected to Ethernet #2 of other Connector	
J3	K-1	ETH 2_TX+	Ethernet Transmit +	Quadrax
J3	K-3	ETH 2_TX-	Ethernet Transmit -	Quadrax
J3	K-2	ETH 2_RX+	Ethernet Receive +	Quadrax
J3	K-4	ETH 2_RX-	Ethernet Receive -	Quadrax
J3	K-S	ETH 2_SH	Ethernet Shield	Quadrax
J3		Ethernet #3	Aux (e.g., to display unit)	
J3	A-1	ETH 3_TX+	Ethernet Transmit +	Quadrax
J3	A-3	ETH 3_TX-	Ethernet Transmit -	Quadrax
J3	A-2	ETH 3_RX+	Ethernet Receive +	Quadrax
J3	A-4	ETH 3_RX-	Ethernet Receive -	Quadrax
J3	A-S	ETH 3_SH	Ethernet Shield	Quadrax
J3		RS-422	RS-422 full duplex interface	

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J3	S-2	RS422_RXD+	Receive Data +	Quadrax
J3	S-4	RS422_RXD-	Receive Data -	Quadrax
J3	S-1	RS422_TXD+	Transmit Data +	Quadrax
J3	S-3	RS422_TXD-	Transmit Data -	Quadrax
J3	S-S	RS422_SH	RS422 Shield	Quadrax
J3		RS232-2	send/receive only	
J3	T	RS232_2_TX	Transmit Data	22D
J3	U	RS232_2_RX	Receive Data	22D
J3	a	RS232_2_GND	RS-232 Return	22D
J3		RS232-1	including flow control	
J3	p	RS232_1_TX	Transmit Data	22D
J3	w	RS232_1_RX	Receive Data	22D
J3	g	RS232_1_CTS	Clear To Send	22D
J3	v	RS232_1_RTS	Ready To Send	22D
J3	m	RS232_1_DCD	Data Carrier Detect	22D
J3	k	RS232_1_DSR	Data Set Ready	22D
J3	h	RS232_1_DTR	Data Terminal Ready	22D
J3	u	RS232_1_RI	Ring Indicator	22D
J3	n	RS232_1_GND	RS-232 Return	22D
J3		Cross Video_RX	Cross Video Receive (LVDS or DVI)	
J3	K-1	X_FP_D0+_RX	Cross LCD flat panel data line 0 (R2-7,G2) RX	Quadrax
J3	K-3	X_FP_D0-_RX	Cross LCD flat panel data line 0 (R2-7,G2) RX	Quadrax
J3	K-2	X_FP_D1+_RX	Cross LCD flat panel data line 1 (G3-7,B2-3) RX	Quadrax
J3	K-4	X_FP_D1-_RX	Cross LCD flat panel data line 1 (G3-7,B2-3) RX	Quadrax
J3	K-S	X_D1_SH	Shield	Quadrax
J3	N-1	X_FP_D2+_RX	Cross LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE) RX	Quadrax
J3	N-3	X_FP_D2-_RX	Cross LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE) RX	Quadrax
J3	N-2	X_FP_CLK+_RX	Cross LCD flat panel Clock RX	Quadrax
J3	N-4	X_FP_CLK-_RX	Cross LCD flat panel Clock RX	Quadrax
J3	N-S	X_D2_SH	Shield	Quadrax
J3	K-1	X_TDMS_D0+_RX	Cross DVI Data Line 0_RX	Quadrax
J3	K-3	X_TDMS_D0-_RX	Cross DVI Data Line 0_RX	Quadrax
J3	K-2	X_TDMS_D1+_RX	Cross DVI Data Line 1_RX	Quadrax
J3	K-4	X_TDMS_D1-_RX	Cross DVI Data Line 1_RX	Quadrax
J3	K-S	X_D1_SH	Shield	Quadrax
J3	N-1	X_TDMS_D2+_RX	Cross DVI Data Line 2_RX	Quadrax
J3	N-3	X_TDMS_D2-_RX	Cross DVI Data Line 2_RX	Quadrax
J3	N-2	X_TDMS_CLK+_RX	Cross DVI Clock_RX	Quadrax
J3	N-4	X_TDMS_CLK-_RX	Cross DVI Clock_RX	Quadrax
J3	N-S	X_D2_SH	Shield	Quadrax
J3		Cross_Video TX	Cross Video Transmit (LVDS or DVI)	
J3	D-1	X_FP_D0+_TX	Cross LCD Flat Panel Data Line 0 (R2-7,G2) TX	Quadrax
J3	D-3	X_FP_D0-_TX	Cross LCD Flat Panel Data Line 0 (R2-7,G2) TX	Quadrax

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Connector	Location	Abbrev	Description	Type
J3	D-2	X_FP_D1+_TX	Cross LCD Flat Panel Data Line 1 (G3-7,B2-3) TX	Quadrax
J3	D-4	X_FP_D1-_TX	Cross LCD Flat Panel Data Line 1 (G3-7,B2-3) TX	Quadrax
J3	D-S	X_D1_SH	Shield	Quadrax
J3	G-1	X_FP_D2+_TX	Cross LCD Flat Panel Data Line 2 (B4-7,HSYNC,VSYNC,DE) TX	Quadrax
J3	G-3	X_FP_D2-_TX	Cross LCD Flat Panel Data Line 2 (B4-7,HSYNC,VSYNC,DE) TX	Quadrax
J3	G-2	X_FP_CLK+_TX	Cross LCD Flat Panel Clock TX	Quadrax
J3	G-4	X_FP_CLK-_TX	Cross LCD Flat Panel Clock TX	Quadrax
J3	G-S	X_D2_SH	Shield	Quadrax
J3	D-1	X_TDMS_D0+_TX	Cross DVI Data Line 0_TX	Quadrax
J3	D-3	X_TDMS_D0-_TX	Cross DVI Data Line 0_TX	Quadrax
J3	D-2	X_TDMS_D1+_TX	Cross DVI Data Line 1_TX	Quadrax
J3	D-4	X_TDMS_D1-_TX	Cross DVI Data Line 1_TX	Quadrax
J3	D-S	X_D1_SH	Shield	Quadrax
J3	G-1	X_TDMS_D2+_TX	Cross DVI Data Line 2_TX	Quadrax
J3	G-3	X_TDMS_D2-_TX	Cross DVI Data Line 2_TX	Quadrax
J3	G-2	X_TDMS_CLK+_TX	Cross DVI Clock_TX	Quadrax
J3	G-4	X_TDMS_CLK-_TX	Cross DVI Clock_TX	Quadrax
J3	G-S	X_D2_SH	Shield	Quadrax

Table 4-8 – J4 Connector Description by Signal Function

Connector	Location	Abbrev	Description	Type
J4		Video	DVI or LVDS = 5 twisted pairs = 10 wires	
J4	A-1	FP_D0+	LCD flat panel data line 0 (R2-7,G2)	Quadrax
J4	A-3	FP_D0-	LCD flat panel data line 0 (R2-7,G2)	Quadrax
J4	A-2	FP_D1+	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
J4	A-4	FP_D1-	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
J4	A-S	AS_SH	Shield	Quadrax
J4	D-1	FP_D2+	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
J4	D-3	FP_D2-	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
J4	D-2	FP_D3+	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
J4	D-4	FP_D3-	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
J4	D-S	DS_SH	Shield	Quadrax
J4	G-1	FP_CLK+	LCD flat panel clock	Quadrax
J4	G-3	FP_CLK-	LCD flat panel clock	Quadrax
J4	G-2	FP_D4+	Future LCD flat panel data 4	Quadrax
J4	G-4	FP_D4-	Future LCD flat panel data 4	Quadrax
J4	G-S	GS_SH	Shield	Quadrax
J4	A-1	TMDS_D0+	DVI Data Line 0 NOTE: only single link supported	Quadrax
J4	A-3	TMDS_D0-	DVI Data Line 0	Quadrax
J4	D-1	TMDS_D1+	DVI Data Line 1	Quadrax
J4	D-3	TMDS_D1-	DVI Data Line 1	Quadrax
J4	D-2	TMDS_D2+	DVI Data Line 2	Quadrax
J4	D-4	TMDS_D2-	DVI Data Line 2	Quadrax
J4	D-S	DS_SH	Shield	Quadrax
J4	A-2	TMDS_CLK+	DVI Clock	Quadrax
J4	A-4	TMDS_CLK-	DVI Clock	Quadrax
J4	A-S	AS_SH	Shield	Quadrax
J4	G-1	DDCCLK	DVI Display Bus Clock	Quadrax
J4	G-3	DDCDATA	DVI Display Bus Data	Quadrax
J4		USB_2/PS2_2	Secondary USB device or PS/2	
J4	K-1	USB_2_PWR	USB +5V power (0.5A max)	Quadrax
J4	K-2	USB_2_D+	USB Data + {5m max length}	Quadrax
J4	K-4	USB_2_D-	USB Data - {5m max length}	Quadrax
J4	K-3	USB_2_GND	USB Ground return	Quadrax
J4	K-S	KS_SH	Shield	Quadrax
J4	K-3	PS2_2_CLK	PS2 Device Clock	Quadrax
J4	K-4	PS2_2_DATA	PS2 Device Data	Quadrax
J4	K-1	PS2_2_PWR	PS2 Device Power	Quadrax
J4	K-2	PS2_2_GND	PS2 Device Ground	Quadrax
J4	K-S	KS_SH	Shield	Quadrax
J4		USB_3/PS2_3	Secondary USB device or PS/2	
J4	N-1	USB_3_PWR	USB +5V power (0.5A max)	Quadrax

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J4	N-2	USB_3_D+	USB Data + {5m max length}	Quadrax
J4	N-4	USB_3_D-	USB Data - {5m max length}	Quadrax
J4	N-3	USB_3_GND	USB Ground return	Quadrax
J4	N-S	NS_SH	USB Shield	Quadrax
J4	N-3	PS2_3_CLK	PS2 Device Clock	Quadrax
J4	N-4	PS2_3_DATA	PS2 Device Data	Quadrax
J4	N-1	PS2_3_PWR	PS2 Device Power	Quadrax
J4	N-2	PS2_3_GND	PS2 Device Ground	Quadrax
J4	N-S	NS_SH	PS2 Shield	Quadrax
J4		USB_4/PS2_4	Secondary USB device or PS/2	
J4	S-1	USB_4_PWR	USB +5V power (0.5A max)	Quadrax
J4	S-2	USB_4_D+	USB Data + {5m max length}	Quadrax
J4	S-4	USB_4_D-	USB Data - {5m max length}	Quadrax
J4	S-3	USB_4_GND	USB Ground return	Quadrax
J4	S-S	SS_SH	USB Shield	Quadrax
J4	S-3	PS2_4_CLK	PS2 Device Clock	Quadrax
J4	S-4	PS2_4_DATA	PS2 Device Data	Quadrax
J4	S-1	PS2_4_PWR	PS2 Device Power	Quadrax
J4	S-2	PS2_4_GND	PS2 Device Ground	Quadrax
J4	S-S	SS_SH	PS2 Shield	Quadrax
J4		Reserved	Reserved for aircraft specific discrete	
J4	b	AC_DISC_5	Reserved for aircraft specific discrete	22D
J4	d	AC_DISC_6	Reserved for aircraft specific discrete	22D
J4	q	AC_DISC_7	Reserved for aircraft specific discrete	22D
J4		Reserved	Reserved for aircraft specific use	
J4	r	AC_1	Reserved for aircraft specific use	22D
J4	p	AC_1	Reserved for aircraft specific use	22D
J4	w	AC_1	Reserved for aircraft specific use	22D
J4	n	AC_1	Reserved for aircraft specific use	22D
J4		EFB Lighting	Display lighting, bezel keys lighting, dimming	
J4	e	28Vdc_ANNUN+	28Vdc Annunciator bus	22D
J4	f	28Vdc_ANNUN-	28Vdc Annunciator bus	22D
J4	s	5Vac_ANNUN+	5Vac Annunciator bus	22D
J4	t	5Vac_ANNUN-	5Vac Annunciator bus	22D
J4		DC Power Return	Power from AID to display	
J4	U	DispDCPWR	Power from AID to display	22D
J4	T	DispDCPWR	Power from AID to display	22D
J4	a	DispDCPWR	Power from AID to display	22D
J4	W	DispDCRtn	Power from AID to display	22D
J4	E	DispDCRtn	Power from AID to display	22D
J4	F	DispDCRtn	Power from AID to display	22D
J4		Ground pins	Ground Pins	
J4	B	Ground	Ground	22D
J4	V	Ground	Ground	22D
J4	C	Ground	Ground	22D
J4	J	Ground	Ground	22D
J4	H	Ground	Ground	22D

4.0 COMMON EFB CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J4	c	Ground	Ground	22D
J4	M	Ground	Ground	22D
J4	L	Ground	Ground	22D
J4	P	Ground	Ground	22D
J4	R	Ground	Ground	22D
J4	Z	Ground	Ground	22D
J4		Reserved	Reserved for display use	
J4	v	DISP_1	Reserved for display use	22D
J4	u	DISP_2	Reserved for display use	22D
J4	g	DISP_3	Reserved for display use	22D
J4	m	DISP_4	Reserved for display use	22D
J4	k	DISP_5	Reserved for display use	22D
J4	h	DISP_6	Reserved for display use	22D
J4	Y	DISP_7	Reserved for display use	22D
J4	X	DISP_8	Reserved for display use	22D

APPENDIX A EXAMPLE WIRE TYPES

Table A-1 – Example Wire Types

Signal Type	Conductor Type	Example Wire Types (Equivalents May Be Used)
ARINC 664 Ethernet	Star Quad per ARINC 664 Part 2	ABS 1503KD24 (24 AWG) BMS 13-72T03C04G024 (24 AWG) ECS 422404 (24 AWG) PIC E50424 The wiring connected to the Quadrax inserts should have 1000Base-T capability. On connector J1, Ethernet 1 and 4 may be merged in order to create a single 1000Base-T link.
DVI	Star Quad per ARINC 664 Part 2	ABS 1503KD24 (24 AWG) BMS 13-72T03C04G024 (24 AWG) ECS 422404 (24 AWG) PIC E50424
	5-Pair (TSP – Twisted Shielded Pair)	ECS 3822410A (24 AWG)
LVDS	Star Quad per ARINC 664 Part 2	ABS 1503KD24 (24 AWG)BMS 13-72T03C04G024 (24 AWG) ECS 422404 (24 AWG) PIC E50424 (24 AWG)
	5-Pair (TSP – Twisted Shielded Pair)	ECS 3822410A (24 AWG)
PS/2	Star Quad per ARINC 664 Part 2	ABS 1503KD24 (24 AWG) BMS 13-72T03C04G024 (24 AWG) ECS 422404 (24 AWG) PIC E50424 (24 AWG)
USB	Star Quad per ARINC 664 Part 2	ABS 1503KD24 (24 AWG) BMS 13-72T03C04G024 (24 AWG) ECS 422404 (24 AWG) PIC E50424 (24 AWG)
	USB Cable	ECS 912204 (22 AWG)
RS-232	Twisted Shield Triple	EN2714-013C004F (22 AWG) EN2714-013C002F (24 AWG) BMS 13-48T26C3G024 (24 AWG) (short distance) 24443/9C062X-4(LD) – 100 ohms (long distance) M27500G24SD3T23 (24 AWG) Red Blue Yellow M27500G22SD3T23 (22 AWG) Red Blue Yellow M27500-22SD3T23 (22 AWG) Standard Primary Colors M27500-24SD3T23 (24 AWG) Standard Primary Colors
RS-422	Star Quad per ARINC 664 Part 2	ABS 1503KD24 (24 AWG) BMS 13-72T03C04G024 (24 AWG) ECS 422404 (24 AWG) PIC E50424 (24 AWG)
ARINC 429	Twisted Shield Pair	EN2714-013B004F (22 AWG) BMS 13-48T26C2G022 (22 AWG) M27500G22SDT23 (22 AWG) PIC D620224 ECS 422402 (24 AWG) ECS 522402 (24 AWG)

APPENDIX A
EXAMPLE WIRE TYPES

Signal Type	Conductor Type	Example Wire Types (Equivalents May Be Used)
Discrete	Single Conductor	EN2267-010A004S BMS 13-48T10C1G22 (22 AWG) BMS 13-48T11C1G24 (24 AWG) M22759/34-22-9 (22 AWG)

Note: EFB installations may use twisted shielded pair wire with Quadrax contacts, in place of Star Quad cable with Quadrax contacts. Rules and constraints for terminating twisted shielded pair wire to Quadrax contacts are provided in Appendix I of this document. Detailed assembly processes should only be defined by the system integrator and/or the cable assembly/contact manufacturer.

APPENDIX B CONNECTOR TERMINATION

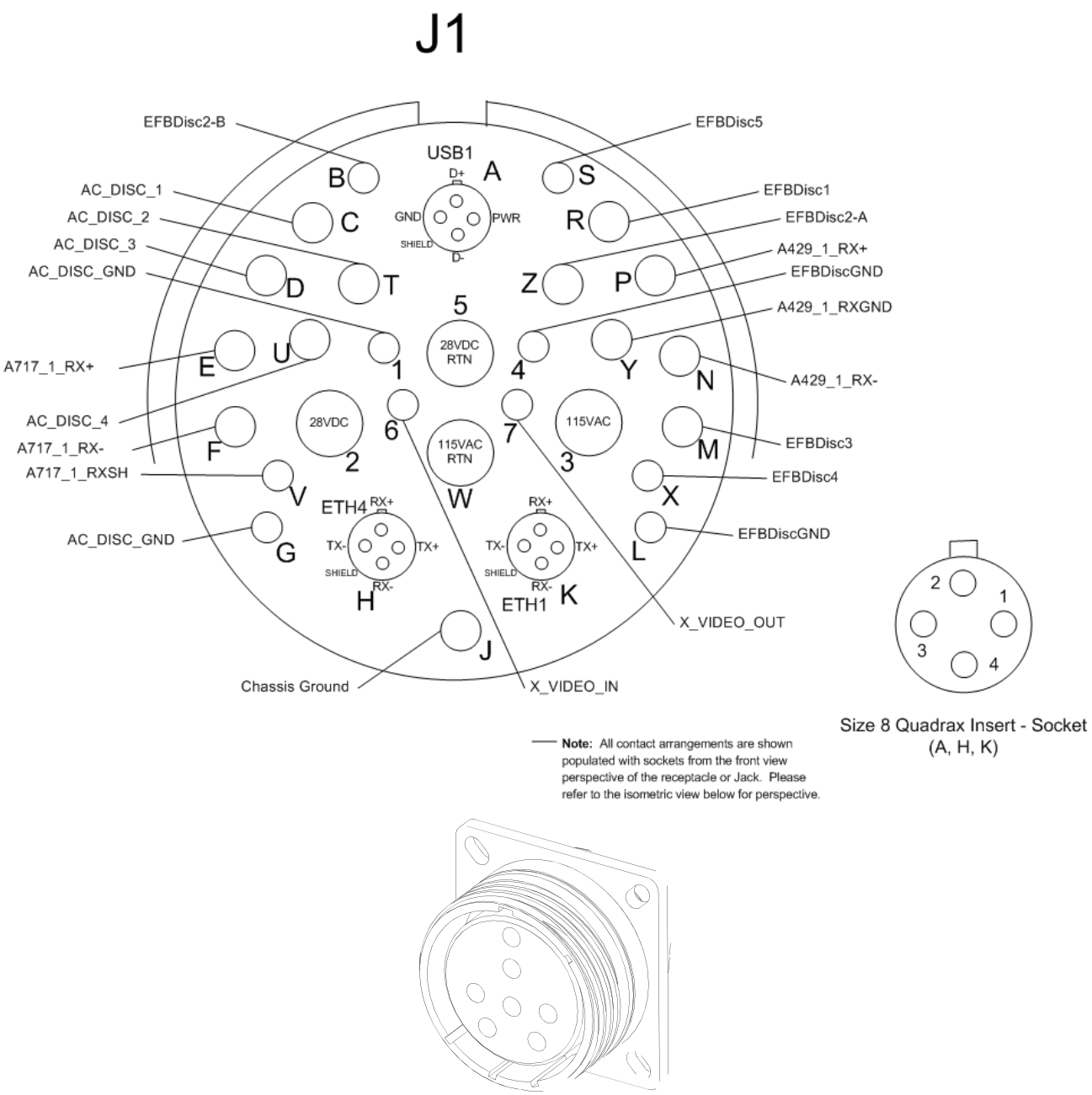


Figure B-1 – J1: EN3645-F0JL20FA

APPENDIX B
CONNECTOR TERMINATION

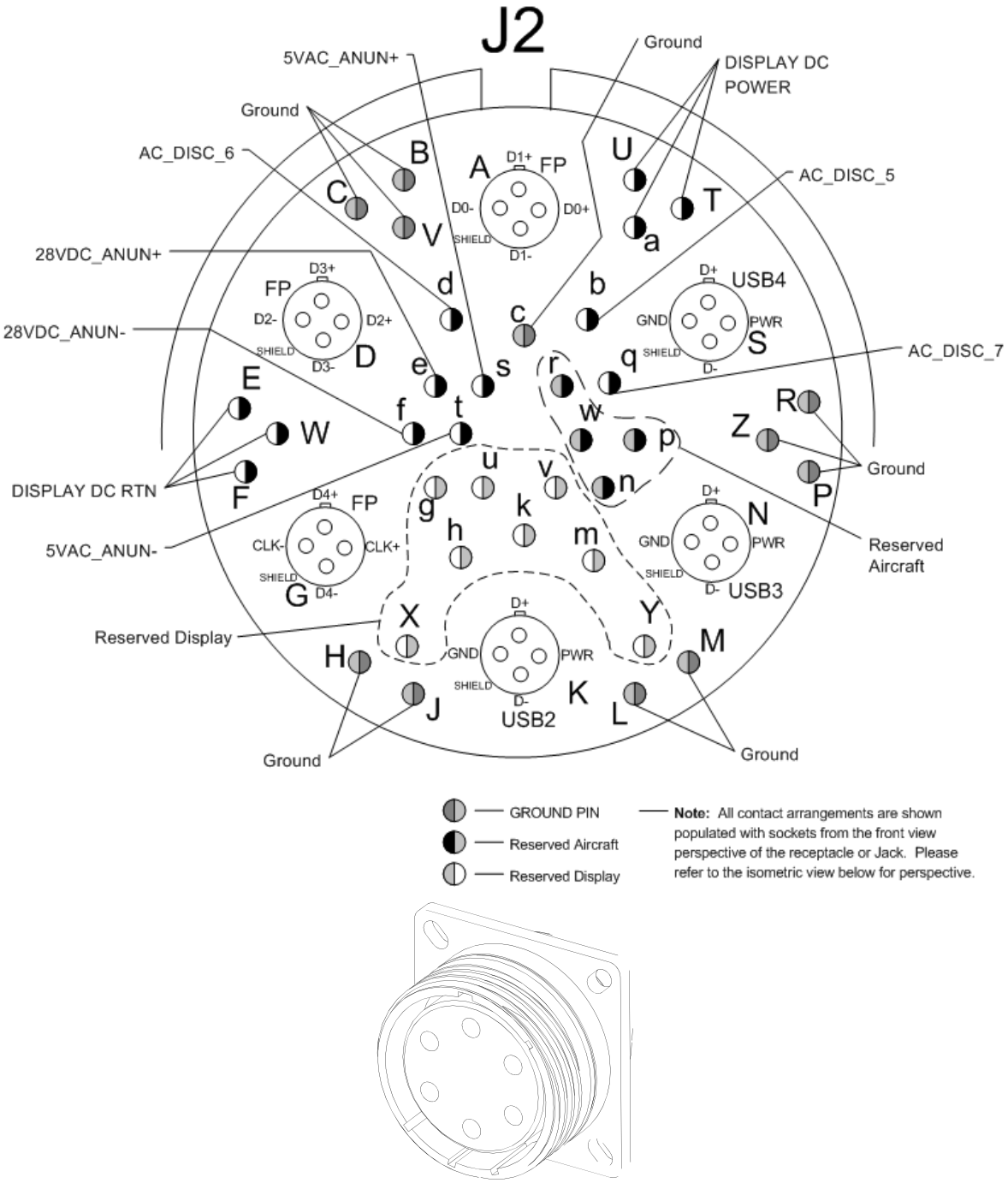


Figure B-2 – J2: EN3645-F0JL17FA

APPENDIX B
CONNECTOR TERMINATION

J3

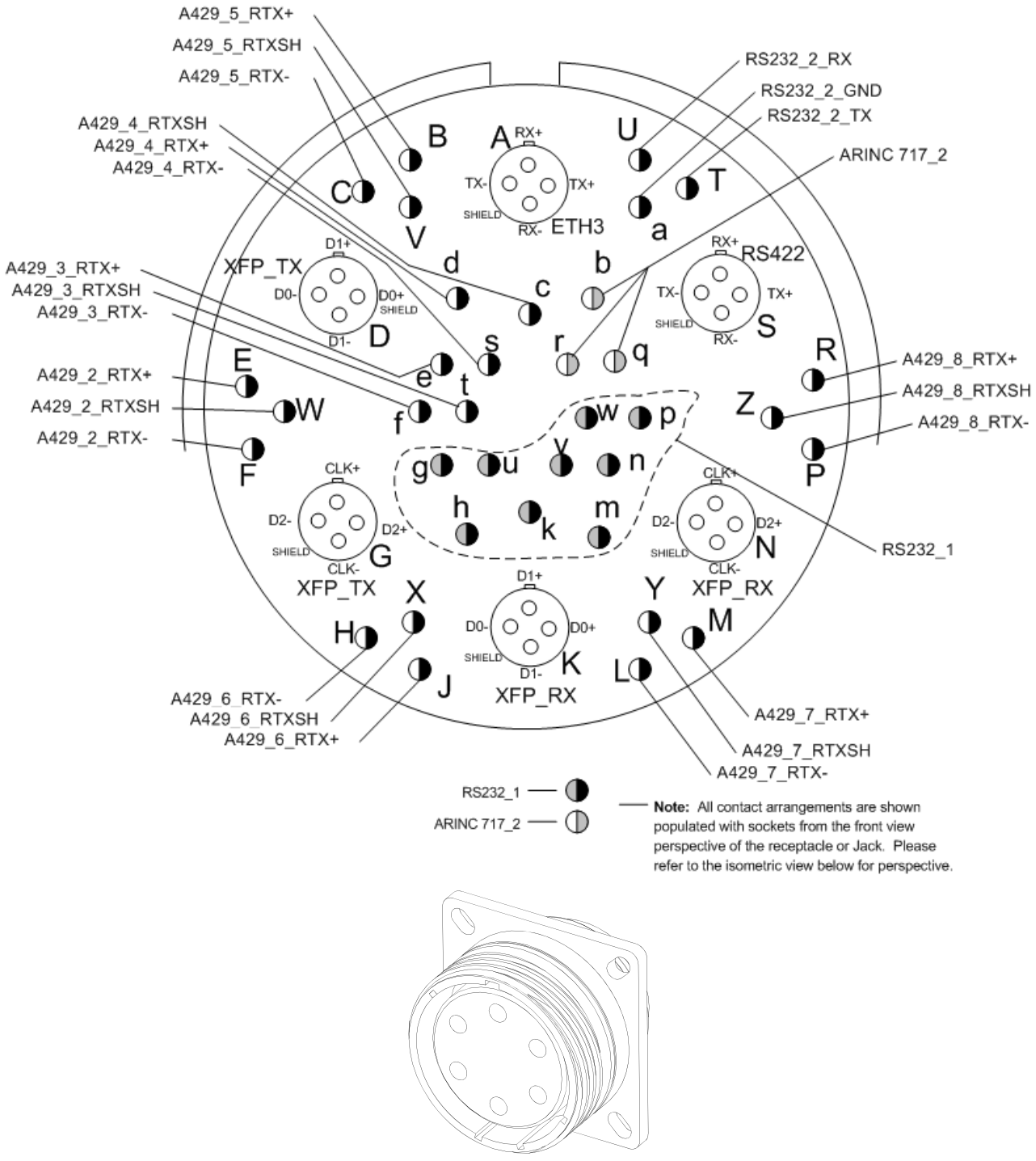


Figure B-3 – J3: EN3645-F0JL17FB

APPENDIX B
CONNECTOR TERMINATION

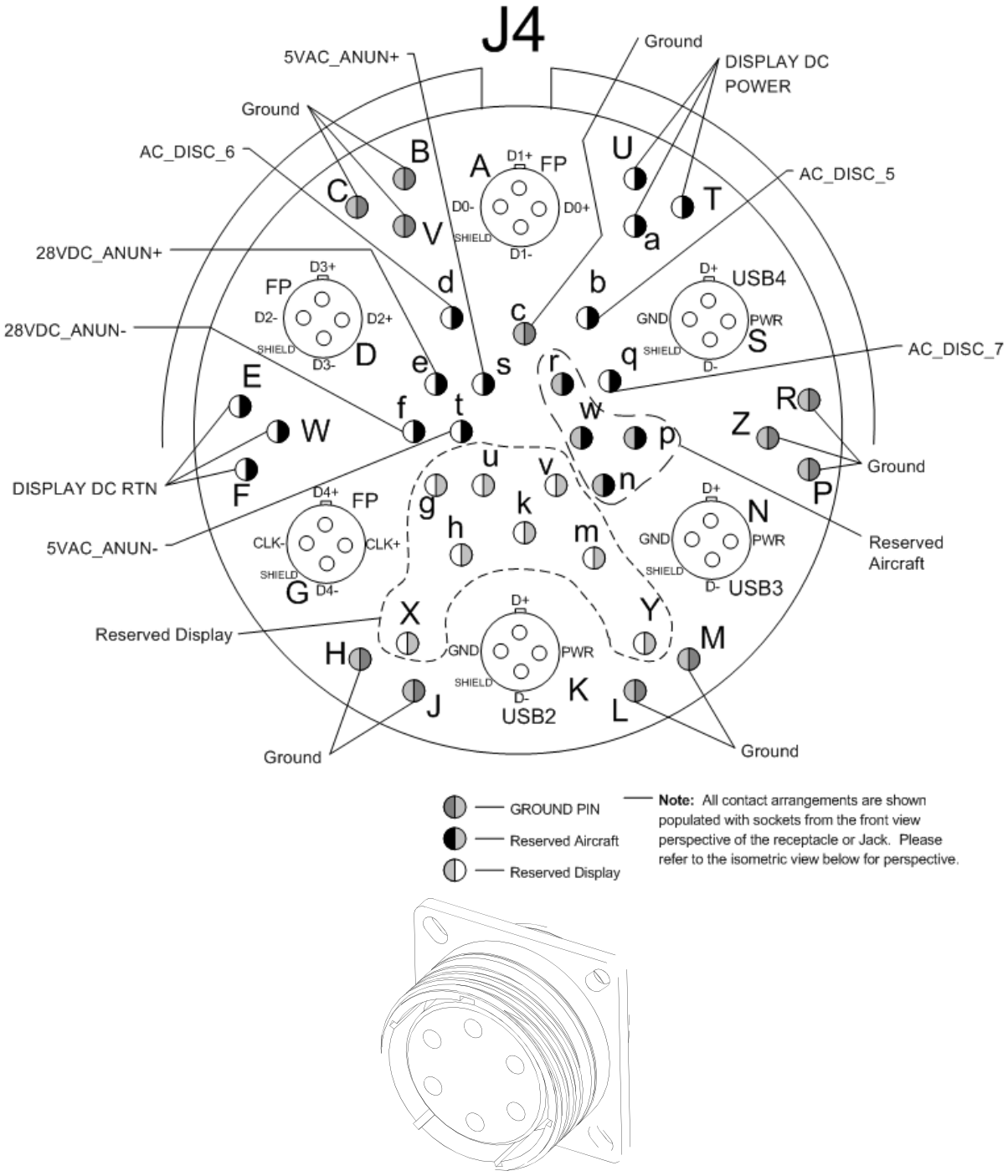


Figure B-4 – J4: EN3645-F0JL17FC

APPENDIX D
AIRCRAFT DISCRETES AND EXAMPLE SIGNAL TYPES

APPENDIX C EXAMPLE USE CASES

This appendix describes eight EFB Use Cases intended as a guide for EFB installers. Color coding for Appendix C:

- Gray is carry-on equipment
- Light blue is equipment being connected to
- Dark blue is OEM installed equipment
- J5 is an alternate for J4 shown in several use cases
- J6 and J7 are alternatives to J1
- Revised use cases utilizing J6 and J7 (in lieu of J1) are illustrated as 1N, 2N, 3N… etc.

Case 1

The aircraft:

- Is equipped with two (dual) instances of J1 or J6 and J7, J2, J3, and J4/J5.
- J2 is wired to J4/J5
- Video signals on J3 are interconnected for video link
- Ethernet signals on J1 are interconnected for data crosstalk
- Aircraft delivers power and discretes only, no data

The EFB:

- Receives power and discretes via J1 or J6 and J7
- Does not use J2, J3, and J4/J5
- Could be a Tablet PC in a docking station within the pilots view
- The AID is part of the docking station
- There is only one EFB

Case 2

The aircraft is equipped in the same way as in case 1.

The EFB:

- Receives power and discretes via J1 or J6 and J7
- Sends data to the other EFB via J1 or J6 and J7
- Sends video signals to the own-side terminal via J2 and J4/J5
- Sends video signals to the off-side terminal via J3 and the off-side AID
- Could contain a Laptop in a docking station outside the pilots view
- The AID is part of the docking station

Case 3

The aircraft is equipped in the same way as in case 1 but in addition sends avionics data to the EFB.

The EFB is the same as in case 2, but the AID is separated from the docking station and the Terminals are not-carry on equipment.

APPENDIX D
AIRCRAFT DISCRETES AND EXAMPLE SIGNAL TYPES

Case 4

The aircraft:

- Is equipped with J1 or J6 and J7only
- The AID functionality and a Network Server Unit are installed in the avionics bay and supply both EFBs with power, discretes and avionics data

The EFB:

- Receives power and avionics data
- Does not use the discretes
- Could be a Tablet PC in a passive (purely mechanical) docking station within the pilots view
- Could exchange data with the NSU
- Could exchange data with the other EFB via the router functionality of the NSU

Case 5

- The aircraft is equipped as in case 3, and
- Uses an integrated OEM terminal to access two EFBPUs installed in the avionics bay.
- A switch allows the pilot to share the integrated OEM terminals between the EFBPUs and the cockpit mounted EFBPUs
- There is no J4/J5
- The EFB is the same as in case 2

Case 6

The aircraft is equipped as in case 5, but:

- Two NSUs supply the EFBs with avionics data and other services
- There is no J3. All avionics data is received via J1 or J6 and J7. Video switching done by other means
- The EFB is the same as in case 2 and 5, except that it does not connect to J3.

Case 7

The aircraft is equipped in the same way as in case 1, but there is a third set of J1 or J6 and J7- J3 connectors shown in the center. Its J2 connector is wired to an OEM Terminal, e.g., for a third pilot in the cockpit or a purser in the forward galley. In this example, the third connector set is not interconnected to the other connectors.

The EFBs shown in the left and right are the same as in case 2.

The EFB in the center is the same, but can not exchange data or video signals with the other two EFBs

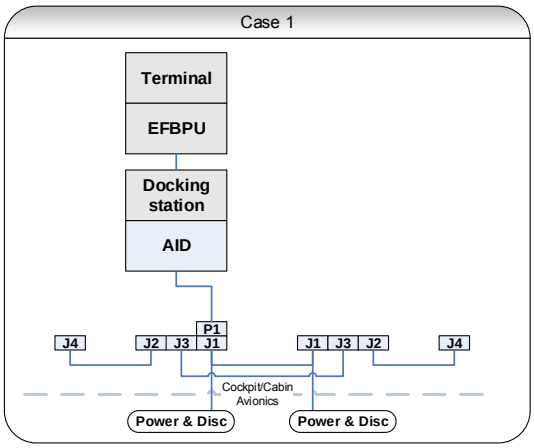
APPENDIX D
AIRCRAFT DISCRETES AND EXAMPLE SIGNAL TYPES

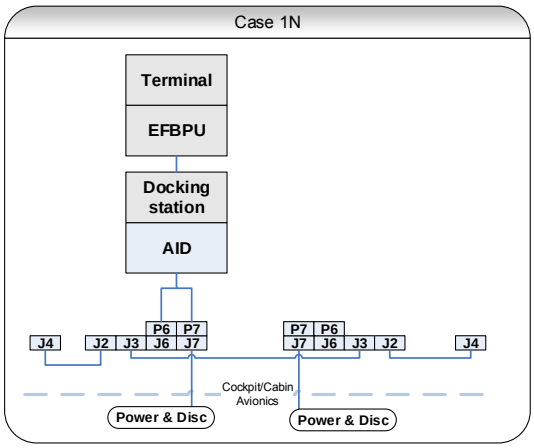
Case 8

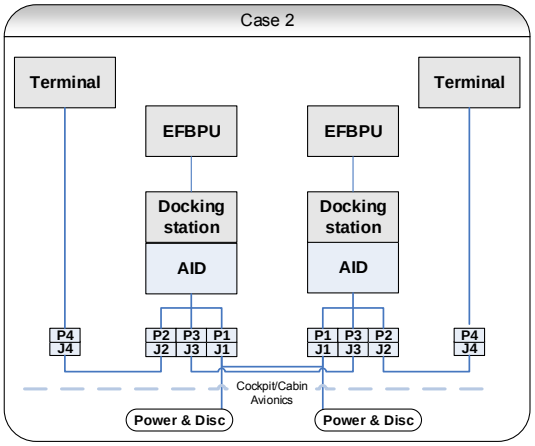
The aircraft is equipped with:

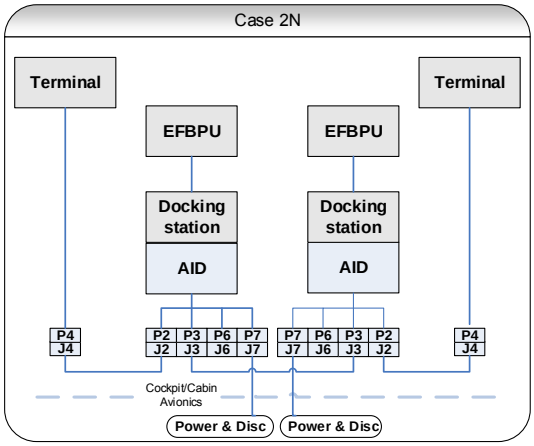
- Four OEM installed terminals, e.g., three in the cockpit and one in the forward galley. They connect to the backside of the J1 or J6 and J7connector, e.g., by transporting video signals via USB.
- Four J1 or J6 and J7connectors, e.g., three in the cockpit and one in the forward galley.
- Four EFBPUs each connected via P1 or P6 and P7 to J1 or J6 and J7. Note that they are no carry-on equipment and therefore do not need an AID.
- Two interconnected Network Server Units which supply avionics data to all four EFBPUs and allow data exchange between them.

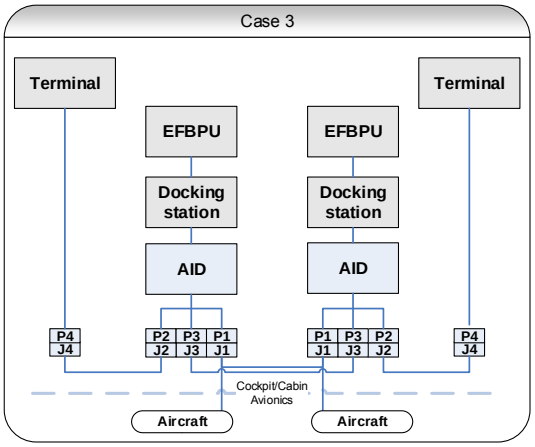
APPENDIX D
AIRCRAFT DISCRETES AND EXAMPLE SIGNAL TYPES

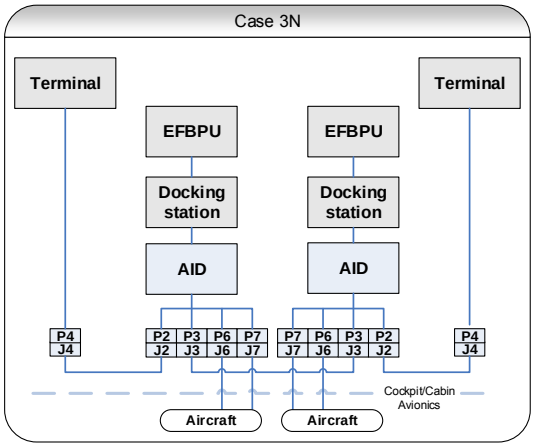




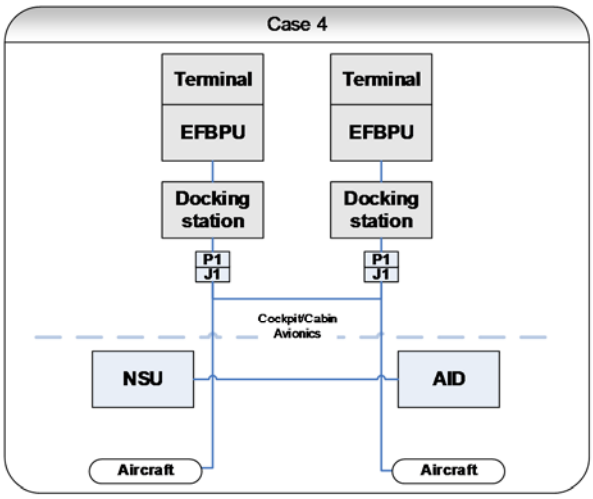


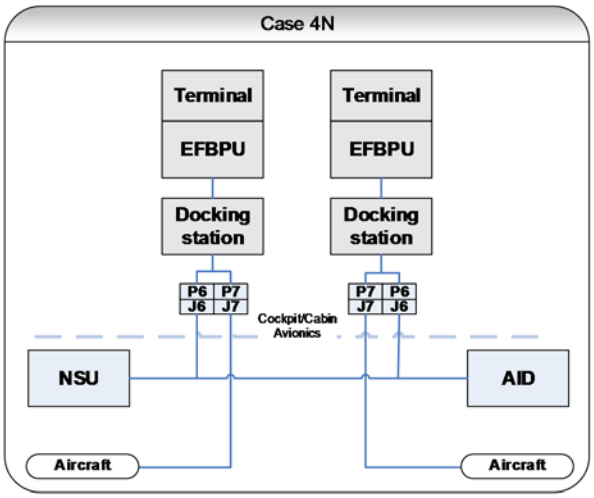


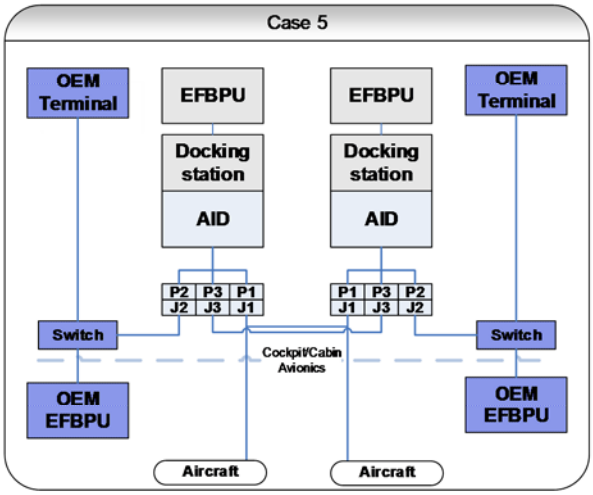


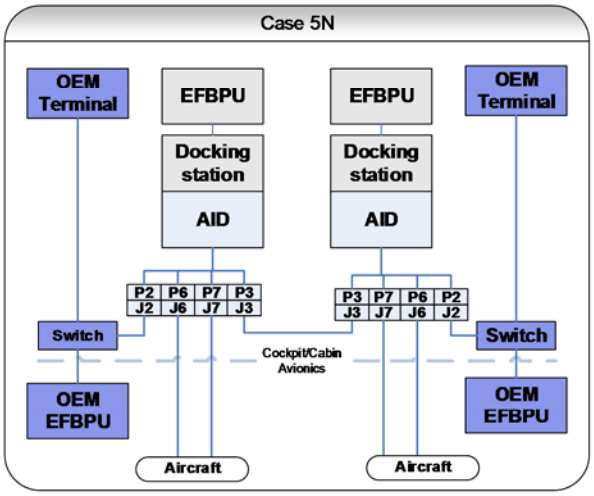


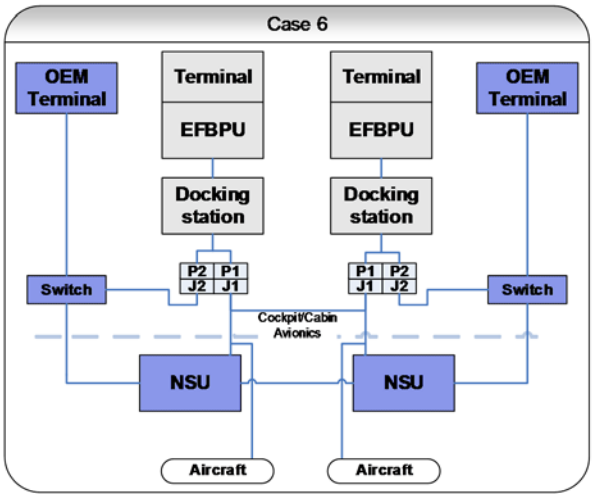
APPENDIX D
AIRCRAFT DISCRETES AND EXAMPLE SIGNAL TYPES

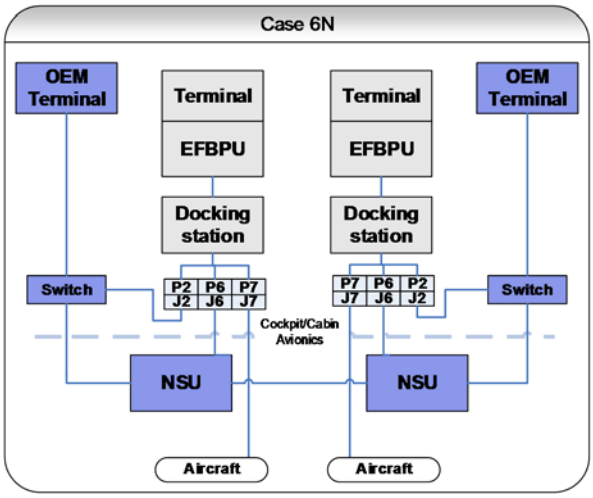




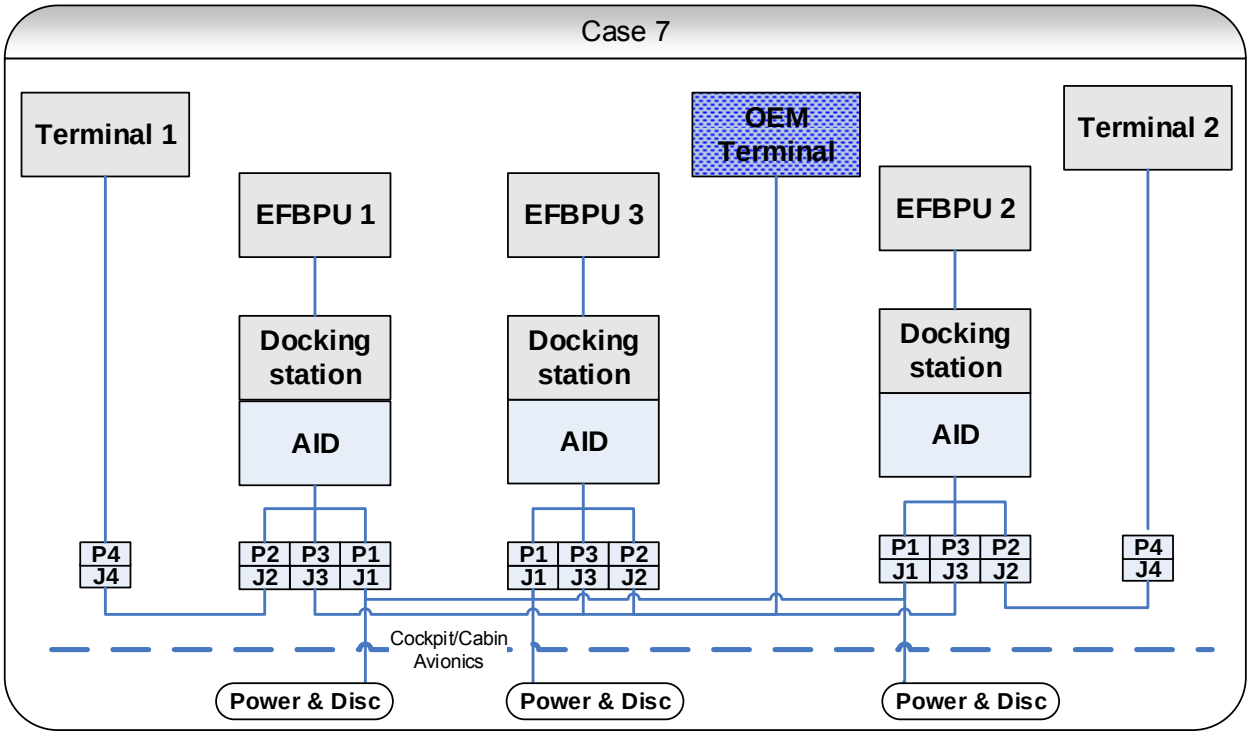


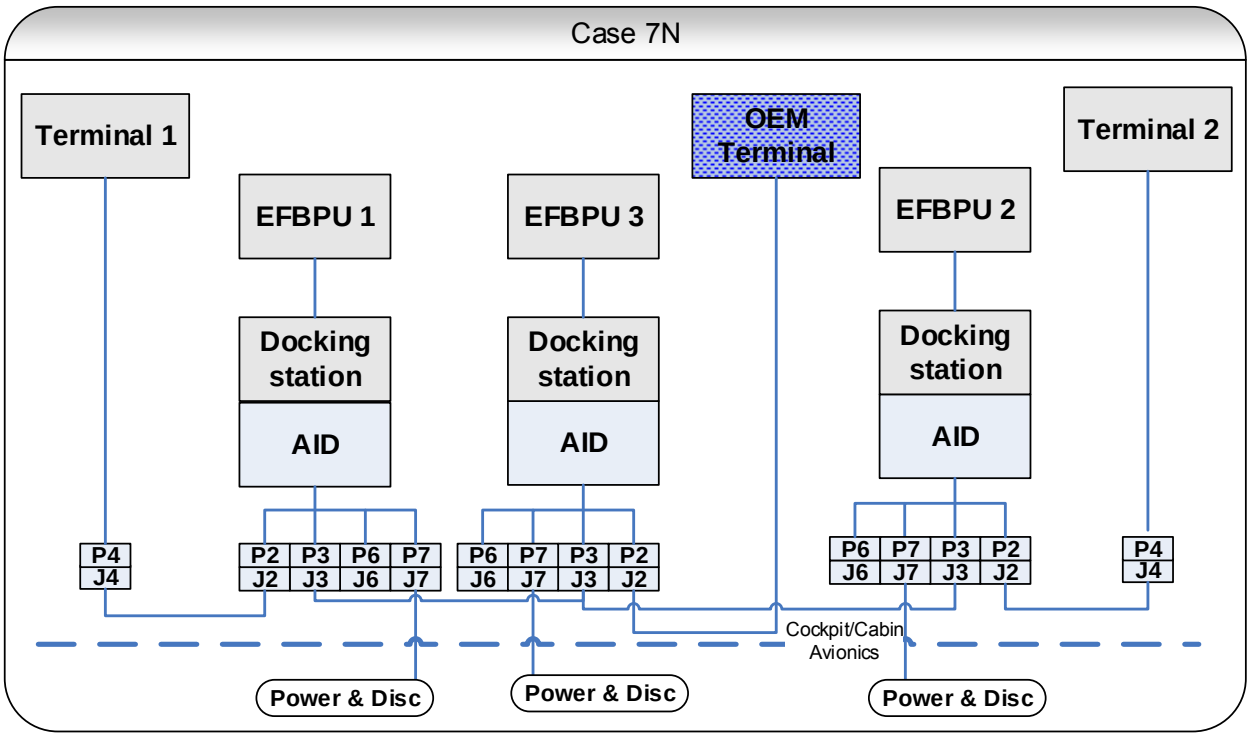




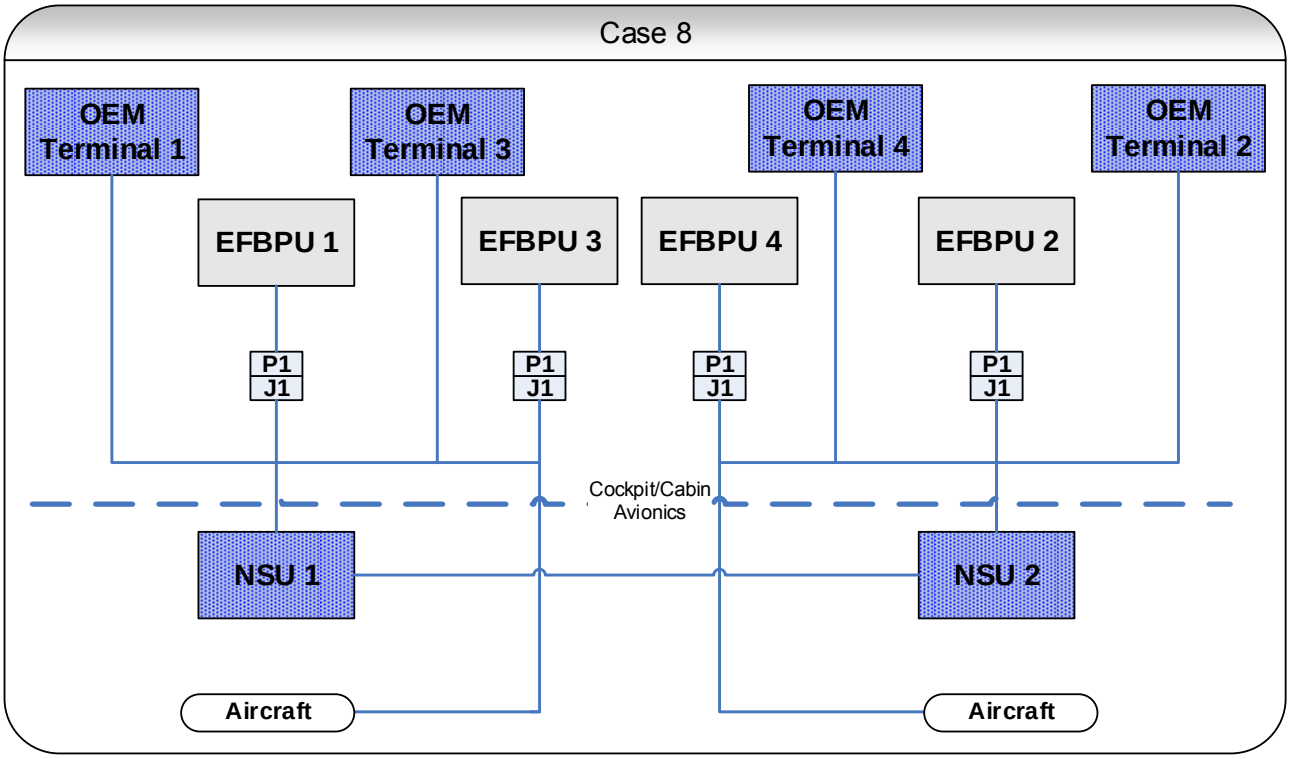


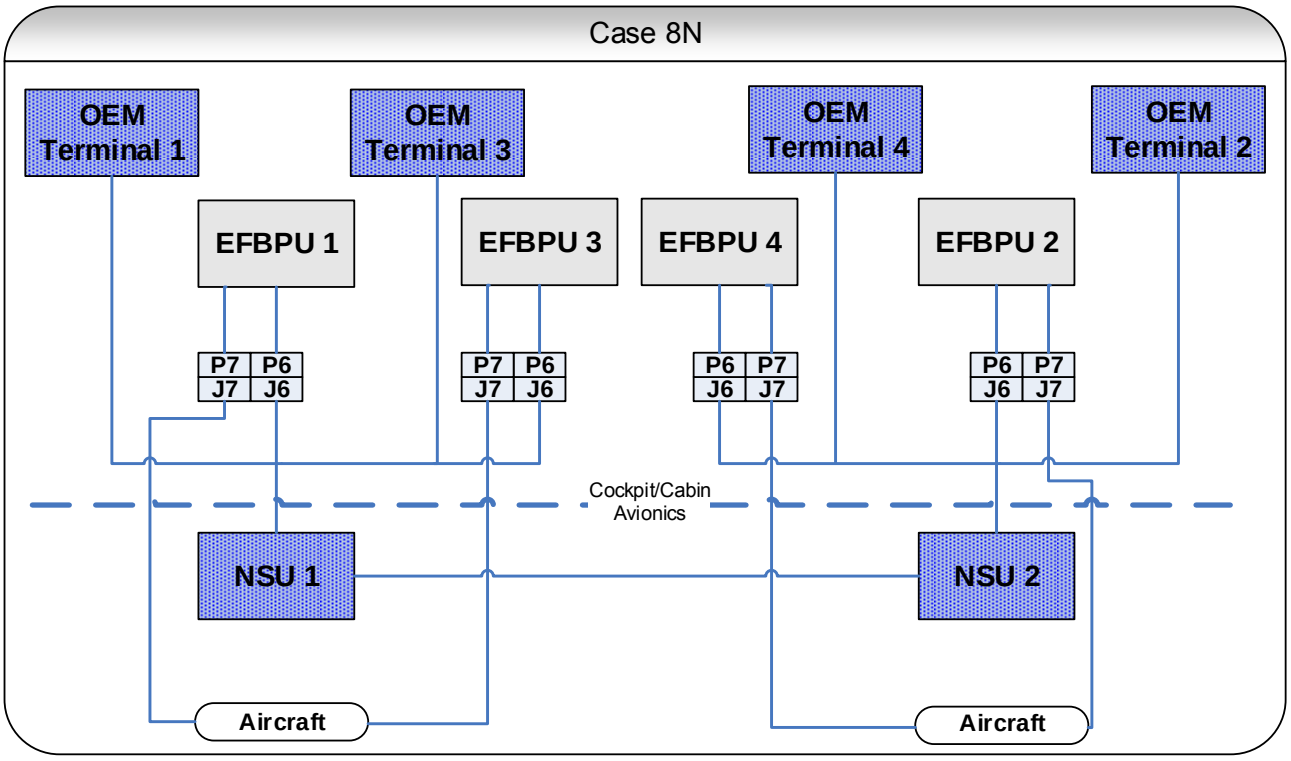
APPENDIX D
AIRCRAFT DISCRETES AND EXAMPLE SIGNAL TYPES





APPENDIX D
AIRCRAFT DISCRETES AND EXAMPLE SIGNAL TYPES





APPENDIX D AIRCRAFT DISCRETES AND EXAMPLE SIGNAL TYPES

The discrete signals listed in this section is for reference only and is not intended to be an all inclusive list, nor is it intended to represent a required list of interfaces. The discretes should be in the form of Power/No-Power, Hi/Lo, Ground/Open, or other "1" or "0" discrete types as defined within Section 0.

COMMENTARY

These discretes could be obtained via digital means from the applicable aircraft systems. However, it should be assumed this will not always be the case. Therefore, the desired "analog discretes" are supported by discrete signal pins in the connector. Digital discretes can be captured via data buses (i.e., ARINC 429, Ethernet, etc.) which are also part of the connector provisioning and only available when power is applied to the aircraft systems.

Table D-1 – Discrete Signals

Pin Name	Commentary
AC_DISC_GND	AC ground can be used for signal guard in pin allocation
AC_DISC_1	WOW (Air/Ground logic) weight on wheels Typically, ground "0" is defined as aircraft on ground.
AC_DISC_2	Aircraft AC/DC Power Available (to know if a certain bus is powered) The Aircraft AC Bus Power Available discrete may be used to determine if aircraft buses are powered from a main power source. This information is needed when the EFB is powered by the ground service bus only. This way, if the EFB is connected to aircraft systems, i.e., ACARS, FMS "listen only," etc., then the EFB will know not to expect those interfaces when main power is down. Basically, the EFB is powered, but the other computers on the aircraft are not. Typically, high "1" identifies the availability of power.
AC_DISC_3 AC_DISC_4 AC_DISC_5 AC_DISC_6 AC_DISC_7	DoorArmed At least one aircraft main door is armed
	EngineStartLeversOn Either engine 1, 2, 3, or 4 start levers have been moved to the "on" position
	EngineXRun Either engine 1, 2, 3, or 4 is running
	ParkingBrakeSet Aircraft parking brake is set or released
	CabinDoorClose
	LandingGearLeverUp
	EngineOilPressureX
	AntiCollisionLightOn
	Custom. Any manufacturer assigned function
EFB_DISC_GND	EFB ground can be used for signal guard in pin allocation
EFB_DISC_1	Reset Discrete from the cockpit to the EFB to initiate an EFB system reset in the event of an application or system hang-up.

APPENDIX D
AIRCRAFT DISCRETES AND EXAMPLE SIGNAL TYPES

<table>
<tr><th>Pin Name</th><th>Commentary</th></tr>
<tr><td>EFB_DISC_2A
EFB_DISC_2B</td><td>Device identification discrete for automatic device configuration
J1-B is Bit 1 (MSB)
where 0=gnd and 1=open
<table>
<tr><th>ID</th><th>MSB J1-B</th><th>LSB J1-Z</th></tr>
<tr><td>EFB_1</td><td>0</td><td>0</td></tr>
<tr><td>EFB_2</td><td>0</td><td>1</td></tr>
<tr><td>EFB_3</td><td>1</td><td>0</td></tr>
<tr><td>EFB_4 to n</td><td>1</td><td>1</td></tr>
</table>
These discretes will allow an EFB to detect its position and set a device name/IP Address. The fourth and all further EFB will not be distinguishable by the two discretes.</td></tr>
<tr><td>EFB_DISC_3</td><td>ShutdownSignal
(On/Off) Discrete from cockpit to enable all power to be removed from the EFB. This discrete will allow the EFB to shut down gracefully.</td></tr>
<tr><td>EFB_DISC_4</td><td>UnitActive
This discrete could provide an activity indicator when there is Ethernet traffic and/or EFBPU processing.</td></tr>
<tr><td>EFB_DISC_5</td><td>UnitPower
This discrete could provide an activity indicator when the EFB is powered. This discrete is used to protect the EFB from draining its batteries completely and to protect it during power transients or abrupt power shutdowns.</td></tr>
<tr><td>X_VIDEO_IN</td><td>Reserved for manufacturer assigned video function. Typically required to signal that the connected AID or EFBPU receives a video signal from the other EFB.
gnd = video send active
open = no cross video transfer</td></tr>
<tr><td>X_VIDEO_OUT</td><td>Reserved for manufacturer assigned video function. Typically required to signal that the connected AID or EFBPU sends a video signal to the other EFB
gnd = video pull active
open = no cross video transfer</td></tr>
</table>

Examples:

Example 1: The EFB may use discrete pin logic Engine 1 run, OR Engine 2 run, AND the air/ground discrete to inhibit the WI-FI.

Example 2: The EFB may use the right front aircraft “door armed” discrete to control the WI-FI on and off.

APPENDIX E EFB SPACE PROVISIONS

E-1 Introduction

For installation of the EFB components on the flight deck, space provisions are required for the EFBPU, connectors, and egress. This appendix specifies a dedicated space for the EFBPU including its associated AID and, if applicable, the docking station and any space which might be required to ensure passive cooling. Therefore, actual equipment size may need to be smaller than the volume available. Additional space is defined for operating and maintaining the EFBPU, i.e. for removing hard discs, laptops, etc.

This appendix specifies maximum dimensions and masses as a guideline for aircraft manufacturers. Of course, any smaller or lighter equipment can be installed.

E-2 EFBPU Space Requirements

For each EFBPU on the flight deck, the following volume may be required. The connections for J1, J2, and J3 will be located on one or multiple of the marked sides.

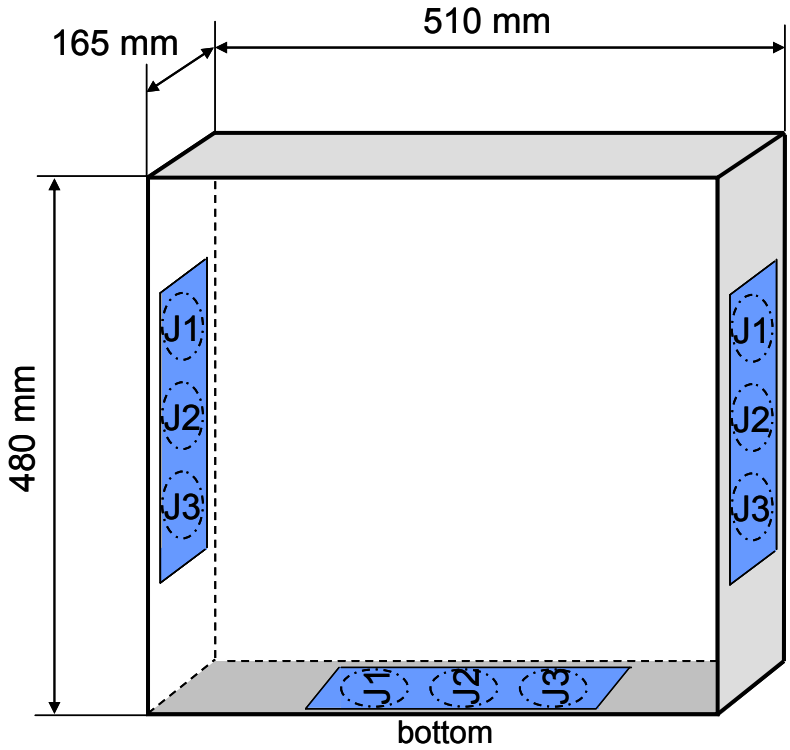


Figure E-1 – EFB Space Requirements

COMMENTARY

Equipment with a volume that is smaller than that specified in this appendix will fit into a wide-variety of airplane types. This volume can be rotated to serve any position needed for the installation. Adequate access to J1, J2, and J3 has to be assured to allow connecting the cables during installation.

APPENDIX E
EFB SPACE PROVISIONS

At the time of this writing, at least one airframe manufacturer has indicated that this volume may not be available on all airplane types. Therefore, EFB suppliers may wish to consider sizes that are within the dimensions: 400mm x 400mm x 100mm.

E-3 EFBPU Additional Space Requirements

Depending on the type of EFBPU to be installed, additional volume may be required for an installation. Additional volume may be needed to gain access to the EFBPU. This volume may be used for changing hard drives, inserting and removing laptops, plugging in USB sticks, etc. This additional space is considered to be optional.

If this additional space is not needed for a particular EFBPU, it may be used for the installation of other equipment. If the space is not viewed to needed, the installer should consider that a change to another EFBPU may require this space. In this case, it shall be easy to obtain the additional space.

This volume is defined as followed:

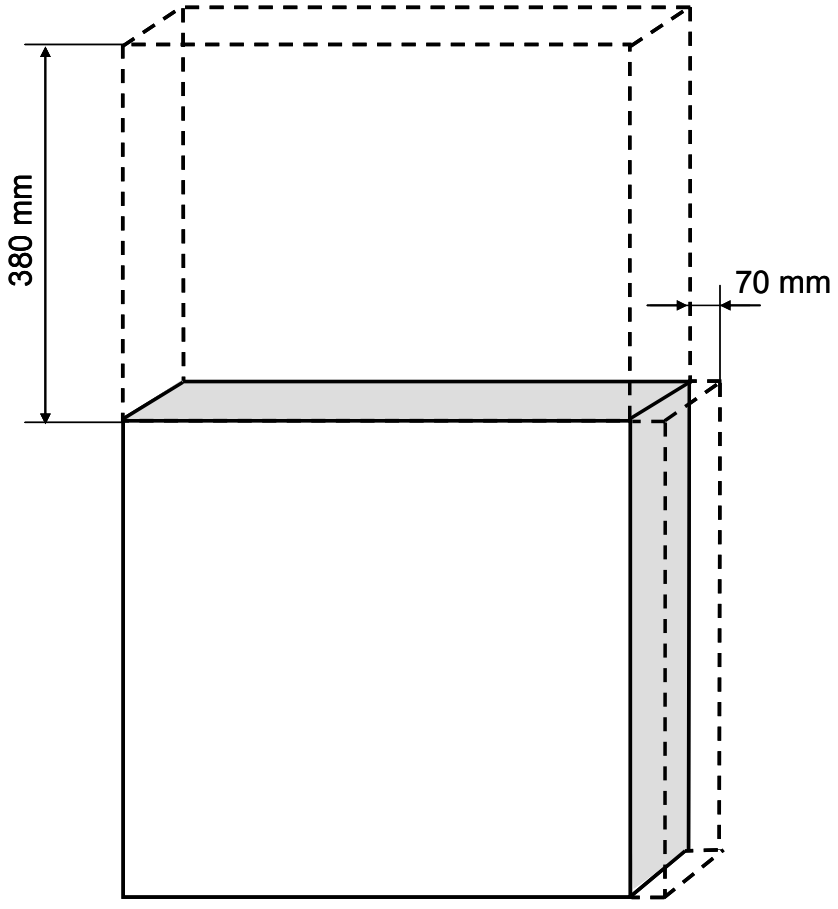


Figure E-2 – EFB Additional Space Requirements

APPENDIX E
EFB SPACE PROVISIONS

COMMENTARY

The additional space does not need to be available during all phases of flight. It could be intruded by an opened door, etc.

If the additional space is smaller it must be easy for pilots and mechanics to clear it if access to the EFBPU is required.

At the time of this writing, at least one airframe manufacturer has indicated that this additional volume may not be available on all airplane types. Therefore, EFB suppliers might consider that overall volume available might be: 150.8mm x 454.8mm x 800mm.

E-4 Maximum Mass and Center of Gravity

The maximum mass of the equipment that occupies this volume (e.g., EFBPU and AID) is 9.1kg.

The airframe manufacturer should consider worst case CG-offset when defining the mounting footprint.

COMMENTARY

At least one airframe manufacturer has indicated that some airplane types may be able to support only 5.5kg. CG-offset may be as much as 240mm ±10mm from the floor.

E-5 Equipment Mounting Footprint

The airframe manufacture should provide a standard mounting footprint for a specific airplane type that supports the EFB envelope defined in ARINC Specification 828.

The EFB installer may be required to use an adaptor plate to attach the EFBPU and/or EFBPU/AID to the aircraft. The attachment points to the adaptor plate are not defined in this standard.

APPENDIX F EFB TERMINAL MOUNTING PROVISIONS

F-1 Introduction

This appendix describes the aircraft and EFB Terminal interface from the perspective of the aircraft sidewall and window frame structural mounting bolt hole pattern. The intent is to provide a standard physical bolt hole pattern interface between a general purpose EFB Terminal mounting bracket/device and factory installed structural mounting provisions.

F-2 Scope

This appendix is intended to define a common aircraft side bolt hole mounting pattern that is installed in the cockpit by the airframe manufacturers at the time of aircraft production. The same mounting pattern may be used by the aircraft owner/operator during an EFB retrofit. This appendix describes the structural interface bolt hole mounting pattern typically required to support the EFB Terminal.

This appendix does not attempt to address the mounting envelope required for various terminals due to the large number of variables related to cockpit controls and user operational preferences.

F-3 Benefit

This appendix is expected to minimize the overall cost to equip an aircraft with an after-market EFB that may utilize a variety of common Terminal devices and mounting brackets. The definition of a common aircraft side, structurally approved mounting bolt pattern provides numerous cost savings benefits such as:

- Allowing the development of standard Terminal mounting brackets
- Allowing end user options between various mounting bracket styles and functionality
- Reduced engineering, installation, and aircraft down time costs when installed at the factory
- Allows use of common hardware across multiple aircraft types

F-4 Bolt Hole Mounting Patterns

The mounting patterns specified by this appendix are intended to be used with ease. Either pattern may be incorporated during aircraft production by the airframe manufacturer and to be adapted to the other pattern or different patterns by the end user with minor effort. Figure F-1 shows a 2.562 inch by 2.250 inch rectangular pattern. Figure F-2 shows a 1.188 inch by 1.50 inch rectangular pattern. Both figures show fore and aft positioning, which allows the two patterns to be overlaid as shown in Figure F-3. This overlay allows for the adaptation of one installed pattern to the other as shown in Figure F-3.

Mounting Pattern A is considered the preferred configuration based upon the larger foot print and the ability to spread the Terminal load over a greater area. The overall area is dimensioned in Figure F-4 for reference.

APPENDIX F
EFB TERMINAL MOUNTING PROVISIONS

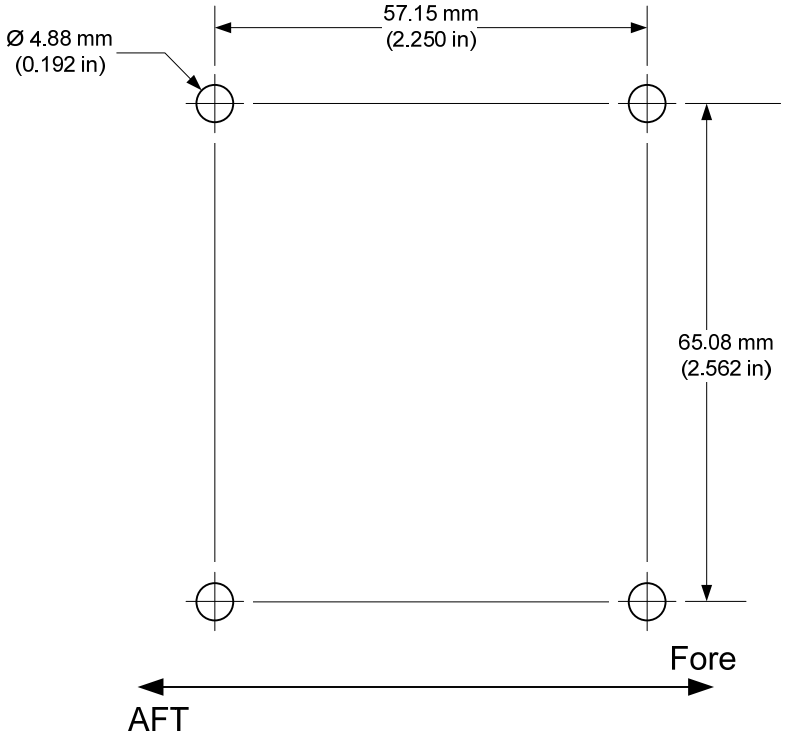


Figure F-1 – Mounting Pattern A

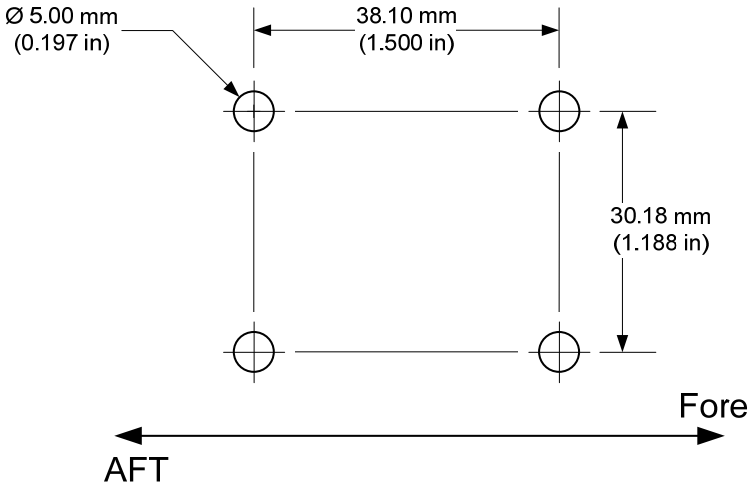


Figure F-2 – Mounting Pattern B

APPENDIX F
EFB TERMINAL MOUNTING PROVISIONS

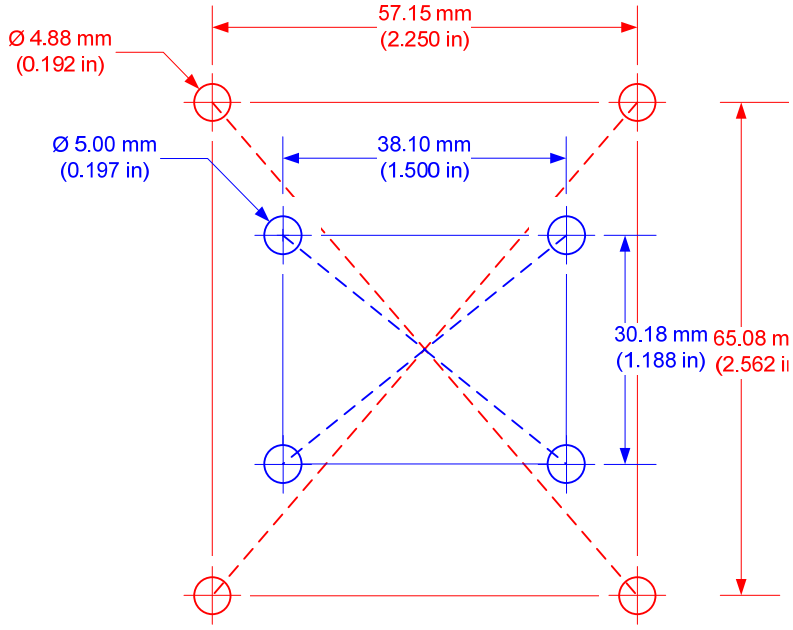


Figure F-3 – Pattern A & B Overlay

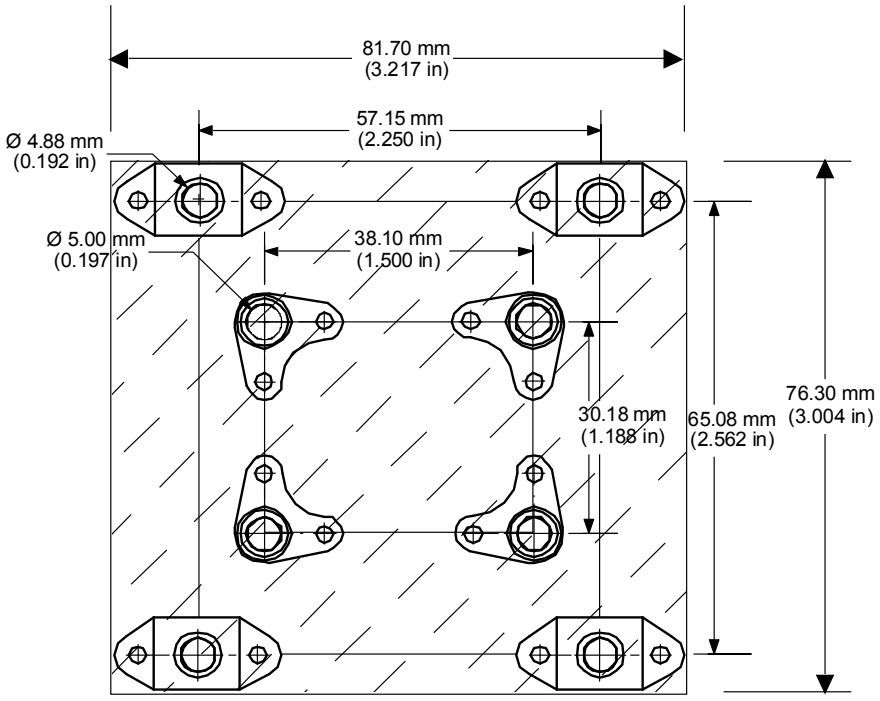


Figure F-4 – Foot Print Area

APPENDIX F
EFB TERMINAL MOUNTING PROVISIONS

F-5 Terminal & Mounting Bracket/Device Weight Considerations

It is necessary to calculate the maximum load for each installation. At the time of this writing, the heaviest Terminal known was 6.7 pounds (3.04 kg). In addition to the direct weight of the Terminal, an additional percentage of weight should be added for CG offset as a result of aircraft mounting. This example shows a terminal, CG offset and example mounting bracket/device:

6.7	Weight of Terminal (lbs)
X.X	Added weight for CG offset (lbs)
1.34	Weight of Mounting Bracket/Device (lbs)
	Total Terminal Weight Considerations

The airframe manufacture and retrofit installation designer may need to take other elements into consideration for the mounting design and limitations.

COMMENTARY

The terminal and mounting bracket weight may be limited to something different than that stated within this document based upon a specific airframe and/or the structure of the base mounting design.

F-6 Mounting Bracket/Device Extension Considerations

The extension of the mounting bracket /device into the cockpit typically limited by the cockpit layout and the ability of the installation designer to restrict the Terminal movement such that it does not interfere with the aircraft controls or egress.

COMMENTARY

The terminal extension may be limited to something different than that stated within this document based upon a specific airframe's terminal base mount design and cockpit control interference. At this time the longest, tested articulating ARM installation known is 8.79 inches (22.33 cm).

APPENDIX G
DIGITAL SIGNAL REFERENCE PLANE, LINK DESIGN, AND VERIFICATION

APPENDIX G DIGITAL SIGNAL REFERENCE PLANE, LINK DESIGN AND VERIFICATION

G-1 LVDS

G-1.1 ARINC 828 LVDS EFB Video Link Overview

The purpose of the LVDS EFB Video link appendix is to define the following:

- ARINC 828 LVDS physical link budget components and performance requirements
- Development Methodology for the Standard ARINC 828 LVDS Link Budget
- Example Calculation of an LVDS Link Budget
- ARINC 828 Aircraft Link Validation Testing methodologies:
  - First of Type (FOT) Installation Designs
  - Line Maintenance Activities

G-1.2 Link Budget Scope and Definitions:

For most use cases, the EFB video link is comprised of the following link segments defined below and illustrated in Figure G-1:

- ARINC 828 LVDS Link Segment
  - J2 to J4/J5 Aircraft Harness
- ARINC 828 EFBPU/AID Link Segment
  - PWB, PWB Connector(s), Internal Interconnects, and EFB PU/AID I/F Cabling
- ARINC 828 EFB Terminal Link Segment
  - PWB, PWB Connector(s), Internal Interconnects, and EFB Terminal Cabling

A link budget modification maybe required when an ARINC 828 EFBPU/AID and/or EFB Terminal Link performs below the basic performance assumptions defined in this appendix.

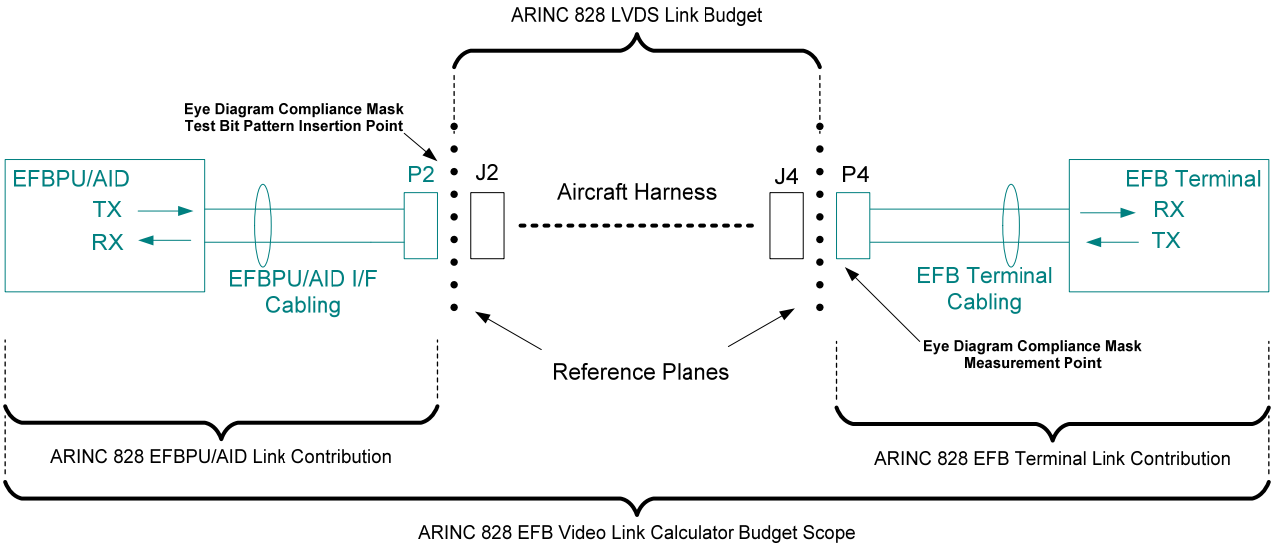


Figure G-1 – EFB LVDS Video Link Components

APPENDIX G
DIGITAL SIGNAL REFERENCE PLANE, LINK DESIGN, AND VERIFICATION

The EFBPU/AID Link and EFB Terminal Link portion of the link consists of everything contained between the LVDS transmitter or receiver device and the EFB side of the connector. This includes internal hardware, such as printed circuit boards, board connectors and over-current or EMI protection devices. The ARINC 828 LVDS link segment consists of all interconnects and cable from the aircraft connector J2 to connector J4/J5 including production breaks.

In the use case of cross-video, there is an additional link segment between the captain's EFBPU and the first officer's EFBPU, connecting J3 to J3. The additional length and production breaks must be considered in the LVDS timing and jitter budgets.

G-1.3 LVDS Link Components and Definition of Significant Characteristics

As a general rule, LVDS link lengths should be kept under 30 ft (9 m) to ensure high signal quality. Each production break within that link will further reduce the working distance. Table G-1 defines the **total** link requirements for an LVDS link in terms of the most significant component characteristics, and includes all tolerance effects such as temperature and frequency.

Table G-1 – LVDS Link Budget Parameters

PARAMETER	UNITS	LIMITS
Differential Impedance	Ohms	100 ± 10%
Insertion Loss (Attenuation)	dB	< 7.96 (at operating frequency)
Capacitive loading (devices + cabling)	pF	< 50 ps/m
Propagation Skew (within pair)	ps	5-20% of t_{ui}
Propagation Skew (pair to pair)	ps	25% of t_{ui}

In addition to these link requirements, it is the responsibility of the EFB supplier to electrically terminate the LVDS transmitter and receiver at 100 Ω differential impedance. It is the responsibility of the EFB system link designer to maximize the differential pair coupling and minimize induced loop currents on adjacent wires by maintaining continuous shielding on the wire pair through production breaks, so that the reference point at each end of the signal path is at a common potential. It is extremely important for link performance that the highest workmanship be used in all wire routing and terminations.

In no case should the link budget choices of the system integrator directly or indirectly mandate use of LVDS devices with capabilities beyond those specified by TIA/EIA-644-A and this standard. If a given link is found to exceed the budget resulting in video performance degradation, and cable lengths cannot be shortened, it is recommended that an LVDS repeater device be introduced that will re-sync the data and clock timing and boost the signal amplitude. Recommendations for integration of a repeater device are beyond the scope of this standard.

G-1.4 Industry Standards for LVDS and Eye Diagram Compliance Masks

Transmitter/Receiver Requirements: TIA/EIA-644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" defines the requirements for the transmitter/receiver IC devices as shown in Table G-2 below:

Table G-2 – LVDS Transmitter and Receiver Requirements

TRANSMITTER SIGNAL PARAMETER	Min	Max	Unit
$\|V_{ODH}\|$ (Differential Output Voltage - High)	250	450	$mV_{0\text{-}pk}$
t_r, t_f (Rise and Fall Time (20% - 80%))	260	$0.3t_{ui}$	ps
t_{jit} (LVDS data path pk-pk jitter)	unspec	Unspec	ps
RECEIVER SIGNAL PARAMETER			
$\|V_{TH}\|$ (Receiver Threshold Voltage)	100		mV
J (typ max allowable jitter)		5%-20% t_{ui}	ps

Voltage level requirements are absolute. Timing requirements are dependent on the bit width or “unit interval”. For example, an LVDS bit rate of 455 Mbps has a data frequency of 227.5 MHz and a unit interval (t_{ui}) of 2.2 ns. This would result in a rise time requirement of 660 ps and jitter requirement in the range of 33-132 ps, dependent on the specific LVDS driver. These requirements define the eye pattern mask for the **differential** voltage, as shown in Figure G-2.

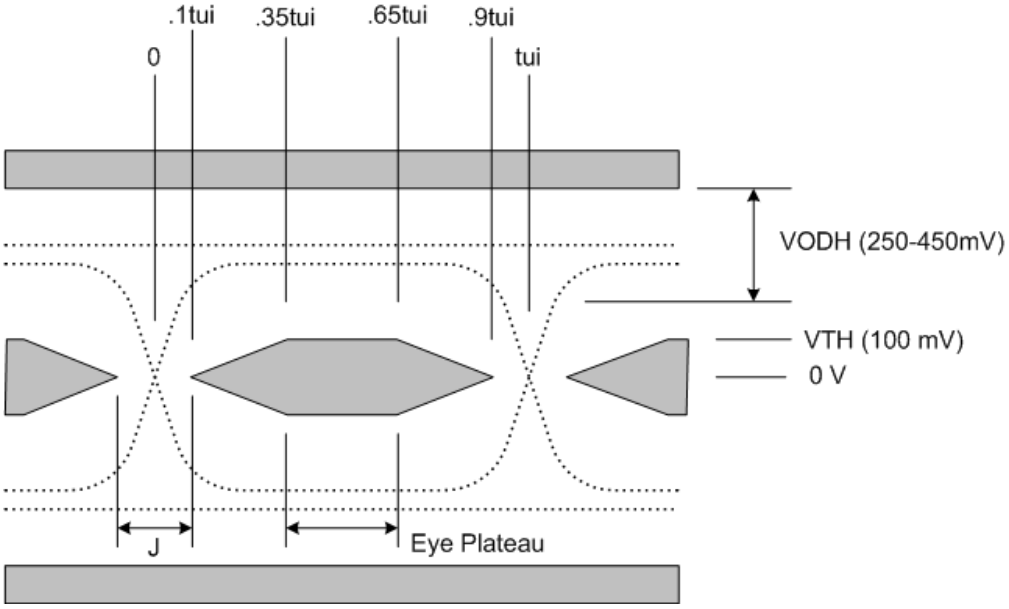


Figure G-2 – LVDS Eye Diagram Compliance Mask at the Device Receiver Pins (Jitter assumed at 20% of t_{ui}, Eye Plateau assumed at 30% of t_{ui})

In addition, the zero-crossing alignment of any data eye pattern to the clock eye pattern should be viewed as significant. IEEE 1596.3-1996 recommends a maximum channel-to-channel offset or “skew” of 600 ps. Therefore, if a clock waveform is overlaid on a data waveform, the zero-crossing of the two waveforms must be horizontally misaligned by no more than 600 ps in either direction.

APPENDIX G
DIGITAL SIGNAL REFERENCE PLANE, LINK DESIGN, AND VERIFICATION

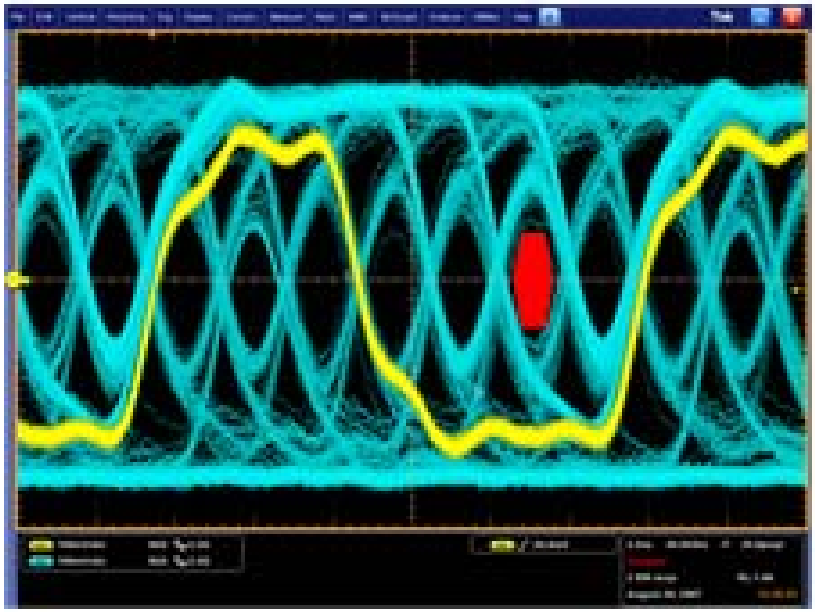
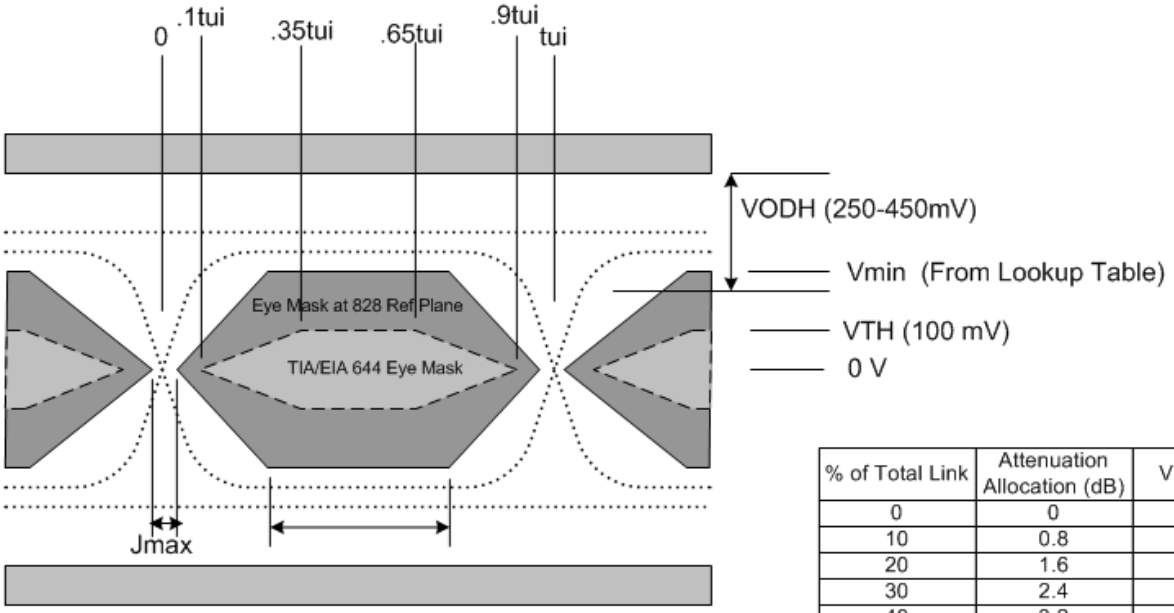


Figure G-3 – Example of LVDS Clock Signal (Yellow) and Compliance Mask (Red) Overlaid on LVDS Data Eye Diagram (Blue)

APPENDIX G
DIGITAL SIGNAL REFERENCE PLANE, LINK DESIGN, AND VERIFICATION

G-1.5 ARINC 828 Link Segment Eye Diagram Compliance Mask

The above eye mask criteria dictate performance at the effective endpoints of the entire physical link. Those total requirements must be budgeted over the entire link length; a portion of the budget allocated to avionics equipment, the remaining portion allocated to the EFB equipment. Since the ARINC Specification 828 portion of the link accounts for a percentage of the total link, the eye mask criteria measured at the aircraft reference points must be scaled accordingly as indicated in Figure G-4.



$$J\max = \%\ of\ Total\ Link \times (0.2tui)$$

% of Total Link	Attenuation Allocation (dB)	Vmin (mV)
0	0	250
10	0.8	228
20	1.6	208
30	2.4	190
40	3.2	174
50	4.0	158
60	4.8	144
70	5.6	131
80	6.4	120
90	7.2	109
100	8.0	100

Figure G-4 – ARINC 828 Link Segment Eye Diagram Compliance Mask

G-1.6 Example of an ARINC 828 LVDS Link Budget Calculation

G-1.6.1 Physical Components of the Link Example

The following link calculation is an example of LVDS video signaling using two cable types; Star Quad and Shielded Twisted Pair. Each cable type has two 2 ft (0.61 m) segments and one 25 ft (7.622 m) segment connected to each other through Quadrax contact terminations.

APPENDIX G
DIGITAL SIGNAL REFERENCE PLANE, LINK DESIGN, AND VERIFICATION

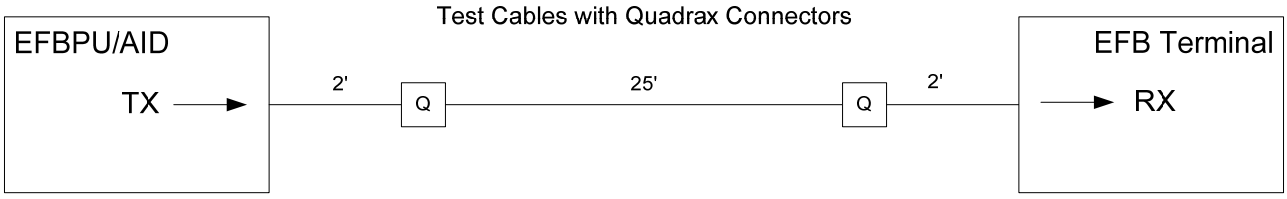


Figure G-5 – EFB LVDS Video Link Example

The available cable and connector properties used in this example are listed in Table G-3 and Table G-4. For any link, the specific cable and connector characteristics must be obtained from the cable supplier.

Table G-3 – Cable Characteristics for LVDS Test Link

Cable Characteristic	Star Quad	Shielded Twisted Pair
Differential Impedance	100 Ω □nominal	100 Ω nominal
Capacitance	49.2 pF/m max	42.0 pF/ft max
Attenuation	0.400 dB/m @ 227 MHz	0.156 dB/m @ 227 MHz
Skew (within pair)	30 ps/m	30 ps/m
Skew (pair to pair)	50 ps/m	50 ps/m
DC Resistance	0.096 Ω/m max	0.079 Ω/m

Table G-4 – Connector Characteristics for LVDS Test Link

Link Characteristics	Quadrax Mated Pair
Differential Impedance	100 Ω
Insertion Loss	0.3 dB @ 100 MHz typical

Excel or another spreadsheet application can be set up to serve as a quick link budget calculator. In the case shown below, unshaded fields are user inputs and the numbered shaded fields are calculated results. Due to the possibility that some aircraft installations may be unique, the installer and/or systems integrator should develop an equivalent calculation using the specific driver/receiver, wire and connector technologies implemented.

Table G-5 – LVDS Link Example: Bit Unit Interval Calculation

Bit Unit Interval	Value	Units
LVDS Clock Frequency	65	MHz
LVDS Data Rate	455	Mbps
1. LVDS Data Frequency	227.5	MHz
2. LVDS Data Unit Interval (t_{ui})	2.2	ns

G-1.6.2 Attenuation (Eye Height) Budget

Using the LVDS transmitter and receiver specifications from the TIA/EIA-644-A, it's a very straightforward calculation of total allowable link attenuation.

$$\alpha_{tot} = 20\log_{10}\frac{V_{TH}}{V_{ODH}} = -20\log_{10}\frac{100mV}{250mV} = -7.959dB$$

In this example, the driver and receiver levels are taken from the IC datasheet, and worst case values are assumed for link budget calculations to yield the most conservative results. The total EFB hardware insertion losses are estimated at 1 dB

at each I/O pin. For greater accuracy, this estimate should be verified through bench test or simulation. Subtracting this and the connector insertion losses give the remaining budget for cabling. Comparing the planned cabling length to the maximum budgeted length yields a PASS/FAIL result, and gives an indication of design margin.

Table G-6 – LVDS Link Example: Attenuation Budget Calculation

Attenuation (Eye Height) Budget	Value	Units	Data Source
Minimum LVDS Transmitter Output	0.270	V	LVDS IC Datasheet
LVDS Receiver Input Threshold	0.100	V	LVDS IC Datasheet
3. Total Attenuation Budget	8.63	dB	= 20log(Vrec/Vtrans)
LRU Allocation	2	dB	Assumption: 1.0 dB at each LRU I/O
Number of Connector Pairs	2		Quadrax contacts per ARINC 828
Connector Loss per Pair (@ data freq)	0.3	dB	Quadrax Datasheet (@ 100MHz)
4. Remaining Attenuation Budget	4.03	dB	
Cable Attenuation (@ data freq)	0.255	dB/m	Test Cable Datasheet (@ 100MHz)
5. Maximum Link Length	15.79	M	
Planned Link Length	8.8	M	29 foot test cable
	PASS		

G-1.6.3 Rise Time & Cable Bandwidth (Eye Opening) Budget

The LVDS driver IC has a finite voltage slew-rate and the datasheet typically provides this information as rise and fall time (t_r and t_f). TIA/EIA-644 specifies that this rise (fall) time not exceed 30% of the bit interval time (t_{ui}).

The capacitive and resistive effects of the cables further impact this rise time and serve as a low-pass filter for the signal, effectively closing the eye pattern opening. While the ANSI and IEEE standards do not specify rise time limitations, there is a minimum eye pattern “plateau width” that the signal must maintain at steady state V_{ODH} before the next transition. This link example estimates that minimum to be 30% of the unit interval.

Additional loading of the LRU equipment “overhead”, such as transient suppression devices for lightning protection, must be included in the calculation.

Table G-7 – LVDS Link Example: Rise Time and Cable Bandwidth Budget Calculation

Rise Time (and Cable Bandwidth) Budget	Value	Units	Data Source
Max Transmitter Output Rise/Fall Time	580	ps	LVDS IC Datasheet
Min Receiver Plateau Width	659	ps	Assumption: 30% of t_{ui}
6. Remaining Rise Time Budget	1538	ps	t_{ui} - min plateau width
LRU Overhead	1.5	pF/line	Transient Suppression Device Datasheet
Cable Capacitance	42	pF/m	Test Cable Datasheet
Cable Resistance	0.096	Ohms/m	Test Cable Datasheet
Planned Link Length	8.8	M	29 foot test cable
7. Cable Bandwidth	255	MHz	Cutoff Frequency = 1/(2*pi* tau)
	PASS		
8. System Rise Time	627.0	ps	Tau = RC
	PASS		

G-1.6.4 Jitter Budget (Eye Width)

ANSI TIA/EIA-644 only provides an acceptable receiver jitter range recommendation based on the data unit interval. Using the liberal end of the range (20% t_{ui}), then subtracting the IC output jitter gives the remaining jitter budget. Dividing the remaining jitter budget by the within-pair skew spec of a particular cable type gives the maximum total length of that cable type before the budget is exceeded. Comparing the planned length to the maximum length yields a PASS/FAIL and gives an indication of link design margin. Great care was taken in terminating the test cables to the Quadrax inserts, therefore in this example connector contributions to within-pair skew are assumed to be negligible.

Table G-8 – LVDS Link Example: Jitter Budget Calculation

Jitter (Eye Width) Budget	Value	Units	Data Source
Max LVDS Output Jitter	190	ps	LVDS IC Datasheet
Max Allowable Jitter at Receiver	440	ps	TIA/EIA-644: 20% of t_{ui}
9. Min Receiver Eye Width Requirement	1.8	ns	For Eye Mask Definition
10. Remaining Jitter Budget	250	ps	
Max Cable Within-Pair Skew	30	ps/m	Test Cable Datasheet
11. Maximum Link Length	8.32	m	
Planned Link Length	8.8	m	29 foot test cable
	FAIL		

G-1.6.5 Timing Budget (Eye Alignment)

IEEE 1596.3-1996 Section 3.4 suggests a channel-to-channel skew limit of ±300 ps for a 2 ns bit width, but lab testing has shown that more is tolerable. Therefore using the assumption that a zero crossing can be delayed as much as 25% of a data unit interval, the driver skew is subtracted to determine the remaining budget allocated to cabling. Dividing this by the maximum pair-to-pair skew of a particular cable type gives the maximum total length of that cable type before the budget is exceeded. Comparing the planned length to the maximum length yields a PASS/FAIL and gives an indication of link design margin.

Table G-9 – LVDS Link Example: Timing Budget Calculation

Timing (Eye Alignment) Budget	Value	Units	Data Source
Max LVDS Output Channel-to-Channel Skew	80	ps	LVDS IC Datasheet
Max Allowable Clk-to-Data Skew	549	ps	Assumption: Timing can be delayed by 25% of t_{ui}
12. Remaining Timing Budget	469	ns	
Max Cable Pair-to-Pair Skew	50	ps/m	Cable Datasheet
13. Maximum Link Length	9.39	m	
Planned Link Length	8.8	m	29 foot test cable
	PASS		

G-1.6.6 Budget Validation through Lab Test

To verify that the cable sets met the calculated link budget performance requirements, they were connected between an LVDS signal generator and a differential oscilloscope on the other. Figure G-6 shows the cable sets connected to the scope.

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Figure G-6 – LVDS Test Cables: Shielded Twisted Pair (Black), Star Quad (Blue)

The green waveforms in Figure G-7 below show the data eye patterns of the cable sets. The yellow waveforms are the LVDS clock signals. Automated measurements to the right of the waveforms show that both cable sets meet the eye diagram compliance mask requirements.

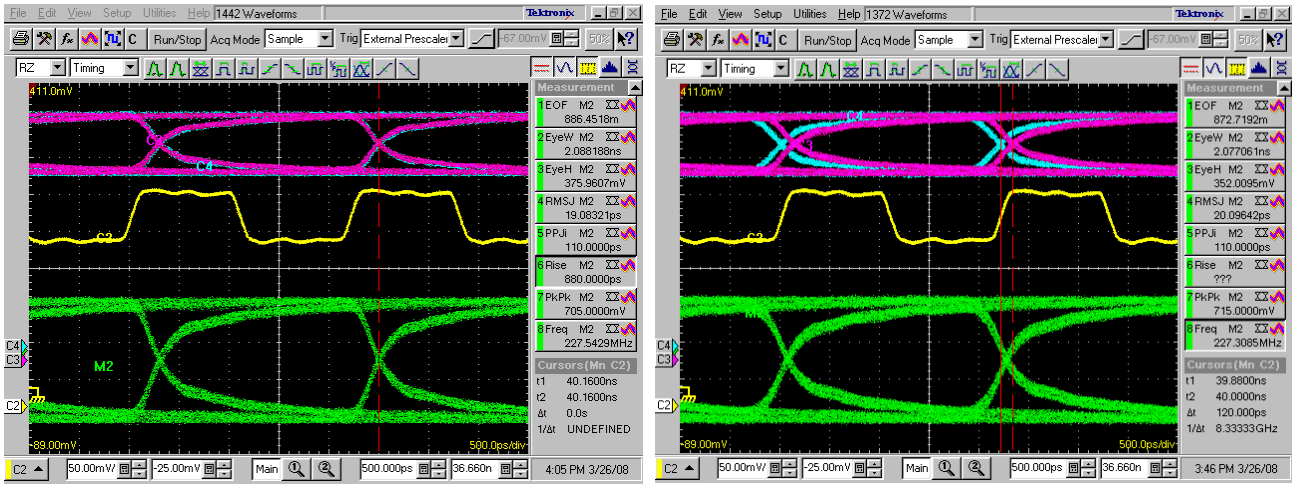

Figure G-7 – LVDS Link Test: Shielded Twisted Pair (Left), Star Quad (Right)

Both cable sets were connected to actual EFB production equipment with a test pattern viewed. No display aberrations were observed with either cable set. (Note: this was Goodrich 8730 Series EBPU and Goodrich 8720 Series EFB DU.)

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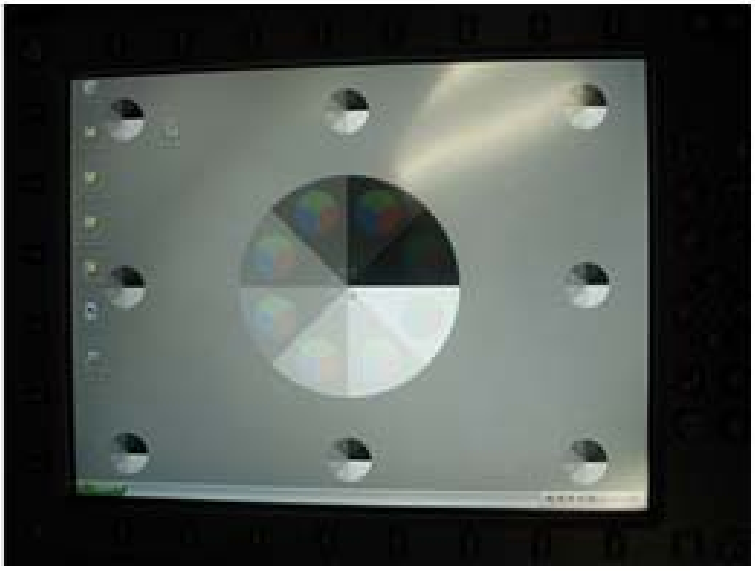

Figure G-8 – LVDS Link Test: Video Test Image

G-1.6.7 Link Budget Example Conclusions

Although the jitter analysis above resulted in a calculated link failure, Table G-9 shows that the planned length only slightly over the maximum calculated length, within 0.5 m. It is very likely that the LVDS transmitter and cable were produced well below the data sheet specification for within-pair skew, performing better than the calculated worst-case jitter. The waveforms in Figure G-7 show eye width measurements of 2 ns, allowing much more margin than calculated.

In all four budgets, it is important to note that any additional cable length, production breaks, or improper terminations or grounding may reduce the margin even further begin to affect the video performance. A cross-video use case will also have additional length to consider.

G-1.7 LVDS Aircraft Link Validation Testing Methodologies

G-1.7.1 First of Type Installation Test

Prior to integrating the EFB system in the aircraft, type testing should be done in a lab with the EFB equipment connected to the installation hardware. If EFB equipment is not available, an LVDS signal generator and an oscilloscope with eye diagram and masking capabilities must be used.

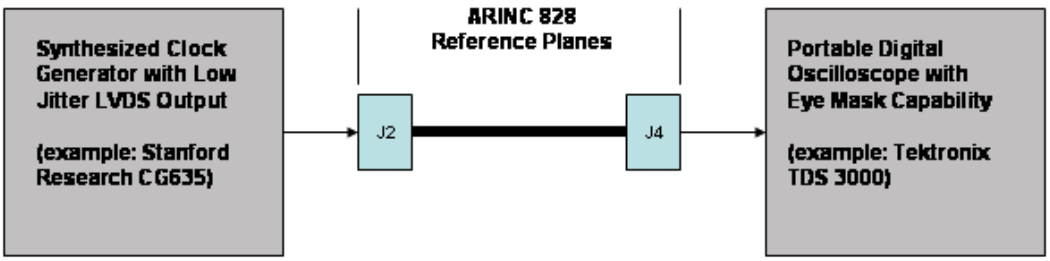

Figure G-9 – FOT Test Configuration

G-1.7.2 Line Maintenance Production Installation Test

For on-aircraft testing of the physical link, the LRUs are typically substituted with portable test equipment similarly to the lab testing, as configured in Figure G-9.

The most effective method of verifying the video link for a production installation or maintenance activity is to display a specified pattern (as shown in Figure G8, for example) and observe the EFB Terminal for visual aberrations or distortion. The best test pattern is one that pushes the limits of the signaling type. Many video quality test patterns are available from VESA (Video Electronics Standards Association) Flat Panel Display Measurement Standard in the public domain https://vesa/sharedwork.com. A recommended pattern for LVDS testing is CINV01.

G-1.7.3 Visual indications of Link Effects

Visual Indications of Link effects may be observe visually. The following list provides a suggestion of parameters that can be observed to qualitatively assess the performance of the EFB LVDS Video Link

1. Lack of display pattern in entirety
2. Pixel dropout
3. Color distortions
4. Loss of edge definition
5. Shadowing
6. Flicker
7. Jitter

G-1.7.4 Fault Isolation Suggestions

If the display were to exhibit any of these artifacts, the first line of defense is to verify end-to-end continuity on all video signal lines. Then look for locations where the pair coupling and/or shielding may be compromised, allowing for noise or cross-talk interference, particularly at production breaks. If the cable terminations are properly done and there are not other likely sources of the signal distortion, then it may be necessary to shorten the cable lengths or add a repeater device.

G-2 DVI

To be added in a future supplement.

G-3 USB

G-3.1 USB Signaling and Link Budget

As illustrated in Figures G-10 and G-11 below, there are two possible cases for the use of the USB 2.0 signals from an EFBPU stand-point: a) between the EFBPU and an aircraft USB 2.0 device, and b) between the EFBPU and a display processing device.

In most cases, the EFBPU is typically acting as a host from a USB 2.0 standpoint and aircraft terminals/end-systems or a display processing device would normally act as a device. For additional topology definition and terminology please refer to USB 2.0 specifications.

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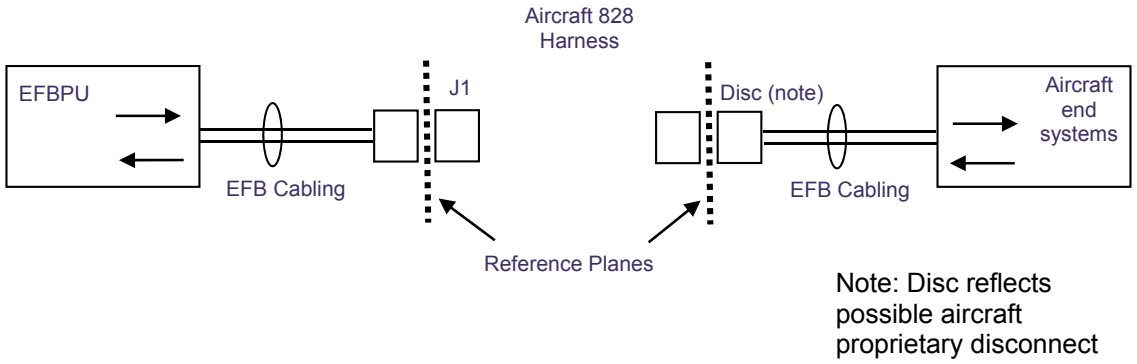

Figure G-10 – EFBPU as Host with Connection to Aircraft End Systems

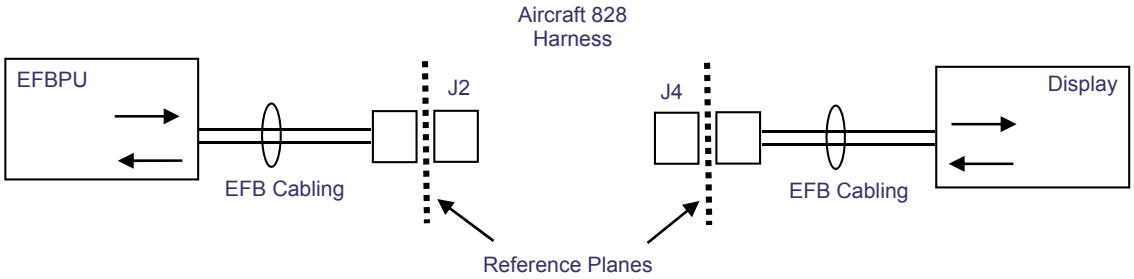

Figure G-11 – EFB as Host with Connection to Display/Terminal (e.g., mouse/keyboard)

The EFB portion of the link consists of everything contained within the EFB between the USB 2.0 root hub and the EFB side of the connector. This includes internal hardware, such as printed circuit boards, board connectors, and over-current or EMI protection devices.

The aircraft portion of the link consists of everything in the link from connector J1 to the aircraft system in scenario (a) and from connector J2 to connector J4/J5 in scenario (b), including production breaks.

Transmitter/Receiver Requirements: USB Specification 2.0 defines in details electrical and timing requirements associated to USB 2.0 transmitters and receivers.

Total Link Requirements: Table G-10 provides a summary of the required cable characteristics associated to links between two USB 2.0 devices. Full specifications are identified in USB 2.0 Specifications and should be used by implementers. It reflects a total link budget for an USB 2.0 link in terms of the link component timing characteristics and includes all tolerance effects such as temperature and frequency.

In addition, it is the responsibility of the EFB supplier to terminate the USB 2.0 transmitter and receiver with suitable terminations and connectors.

Table G-10 – Required Cable Characteristics

Characteristics	USB 2.0 Specification
Cable topology	Shielded twisted pair
DC resistance	< 0.6 Ω
Cable Skew	< 100 ps
Propagation delay: Full/High-speed Low-speed Impedance (Zo)	 < 26 ns < 18 ns 90.0 ±13.5 Ω
Cable Loss: 10 MHz 100 MHz	 < 0.6 dB < 2.0 dB

Refer to section 6.7 of USB 2.0 specification for detailed link requirements.

Notes:

1. A cable length of 15 feet maximum is expected to meet the USB 2.0 specification. For cables specified to support USB 2.0 performance, USB 1.1 host/devices may be able to communicate over a longer distance than 15 feet provided additional propagation delay testing is performed.
2. If a given link is found to exceed this budget, resulting in data transmission performance degradation, and cable lengths cannot be shortened, it is recommended to introduce a USB 2.0 repeater device within the cable assembly.
3. It is important to note that a maximum of seven USB layers as defined in USB 2.0 Specification is allowed including both the host chip and the end device chip.
4. Recommendations for integration of a repeater device are beyond the scope of this standard.

G-3.2 USB 2.0 Bench and On-Aircraft Link Test

For bench tests typically performed on the ground in a lab environment, it is recommended that implementers setup test units representative of end systems in use on aircraft as well as conforming cables and connector arrangements reflecting the intended aircraft installation.

Two sets of tests are recommended:

- Eye diagram tests using COTS data analyzers providing USB 2.0 test capabilities
- USB 2.0 performance tests using off-the-shelf loopback testers validating achieved bandwidth and error rate

For on-aircraft tests, performance tests using off-the-shelf loopback testers validating bandwidth and error rate should be run first on the EFB alone and then at the far end of installation in order to validate link performance.

A bandwidth drop of about 20 Mbps can be assumed by the integrator for each repeater inserted in the link installation.

G-3.2.1 USB 2.0 Test Results on Reference Cable

The following is a summary of USB 2.0 testing performed on the Reference Cable assembled in support of ARINC 828. For more information on the Reference Cable please refer to the introduction of this Appendix G.

The summary test data below is aimed at describing a typical ground-based performance of cables supporting USB 2.0 communications. Two cables sub-assemblies were considered during the USB 2.0 testing. Two types of tests were performed:

- USB data transfer and loopback (error rate) performance using COTS test tools
- Eye diagram verifications

For each test category, a performance baseline was established with a 4-inch long reference ‘short’ cable which is used to validate the test environment in near optimum conditions.

G-3.3 Data Transfer Performance

The data analyzer tool used for data transfer performance tests is called “PassMark.” The PassMark performance test allows the data transfer rates for short bursts of data transfer to be measured on the cable under test.

The test tool generates a block of data (2k bytes in full-speed and 32k bytes in high-speed) from a generating device to the PassMark USB 2.0 device, which will count the number of packets (64-bytes in full-speed and 512-bytes in high-speed) per USB microframe (1ms in full-speed and 125us in high-speed).

It calculates the maximum speed based on these metrics. This is defined as one benchmark operation.

This test is performed ten times, followed by the benchmark of receive speed, where the PC requests a block of data from the PassMark USB 2 device.

This test will be repeated until the test is stopped manually or until the test duration is reached.

Cable 1 characteristics:

- Maximum data rate was 300 Mbps. The minimum data rate was 265 Mbps

Cable 2 characteristics:

- Maximum data rate was 300 Mbps. Average data rate was 294 Mbps

Both cables provides satisfactory performance (i.e. similar to the Reference ref. Cable)

For Loopback/Error Rate performance, the Passmark data test tool was used for the subject error rate/loopback performance tests.

The loopback test is used to verify if the cable causes the signal quality to degrade by verifying if the data sent is the same as the data received.

The PassMark test tools used generates various data packet sizes (64bytes in Full-speed and 512-bytes in High-speed) to the USB device. It loops this data back in firmware and send the same data back to the PC.

For Cable 1, 24 errors were detected over 748 loopbacks. This indicates a **minor issue** associated to signal degradations.

Cable 2 exhibited 105 errors detected over 499 loopbacks. This indicates a **medium issue** with reference to signal degradations.

The reference cable showed no errors over 740 operations

The eye pattern tests are performed using Agilent COTS oscilloscope and associated USB 2.0 test software. This test tool can also be used to verify USB 1.1 operation.

Reference Cable:

The EFB is used to run test software to send data through the cable under test.

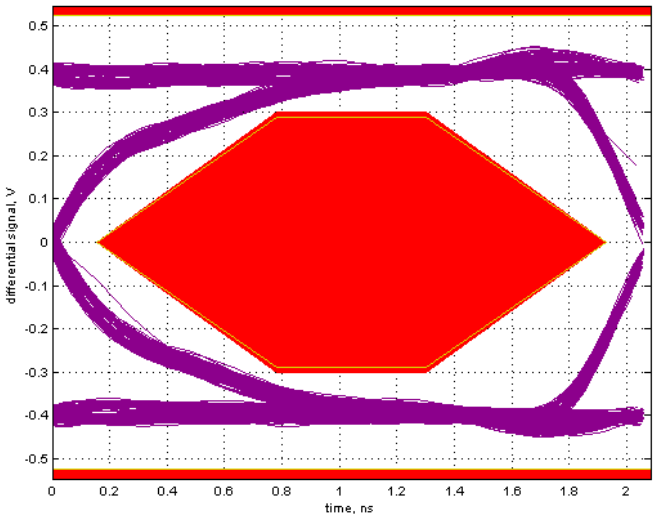

Figure G-12 – Eye Pattern Characterization

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The reference cable is used to calibrate the test data.

Cable 1 results:

With Cable 1, the eye pattern is generally out of the inner eye pattern which indicates propagation and attenuation challenges to the signal. The general pattern generated by the signal is reasonably symmetrical on the other hand.

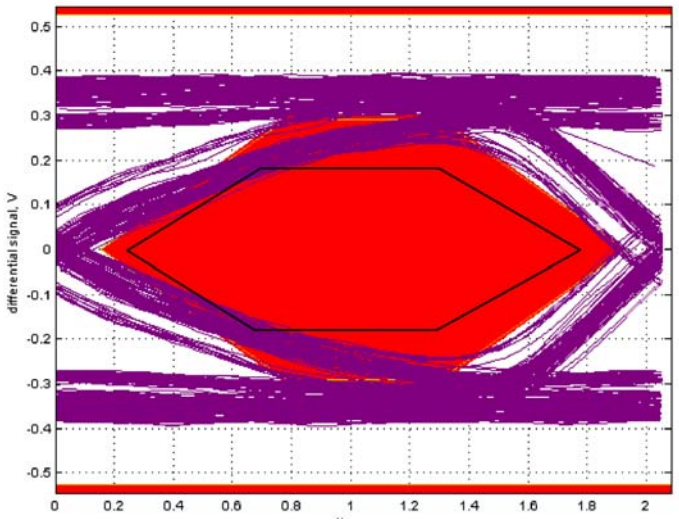

Figure G-13 – Eye Pattern Characterization: Cable 1 Results

Cable 2 results:

Cable 2 exhibits a similar pattern to Cable 1 with no visible improvements or differences. This signal is generally external but very close to the edge of the reference pattern (inner polygon)

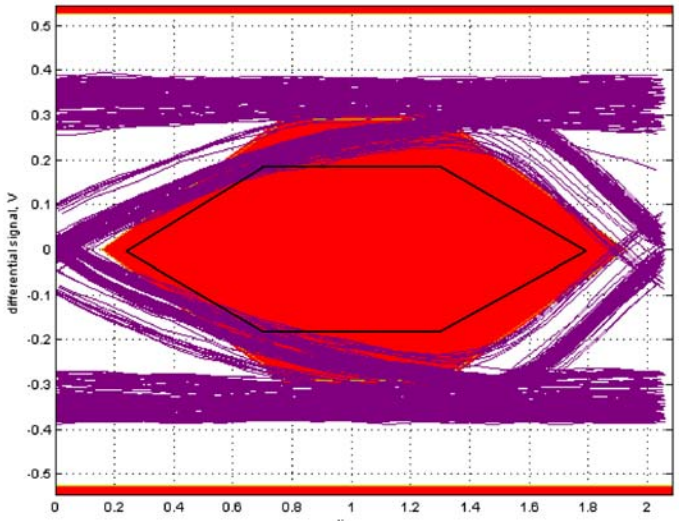

Figure G-14 – Eye Pattern Characterization: Cable 2 Results

Conclusions from sample cable testing:

- Both sample Cable 1 and Cable 2 provide adequate data performance overall.
- While USB 2.0 does not prescribe length, cable loss and propagation delays, these affect significantly signal quality as illustrated by the eye diagrams shown above.
- The cables under test may exhibit USB performance issues under certain environmental conditions or depending on the USB 2.0 end-system characteristics which may vary from one supplier to another.
- Limiting the cable length to less than 5m should address these issues.

A summary of the characteristics measured on the cables is provided below.

Table G-11 – Cable Characteristics

Characteristics	USB Specification	Cable 1	Cable 2
Cable Topology	Shielded Twisted Pair	Shielded Twisted Pair	Shielded Pair Only
DC Resistance	< 0.6 Ω	0.6 Ω	0.73 Ω
Cable Skew	< 100 ps	381 ps	n/a
Propagation Delay: Full/High-Speed Low-Speed	 < 26 ns < 18 ns	 n/a n/a	 n/a n/a
Impedance (Zo)	90.0 ± 13.5 Ω	100 ± 10 Ω	100 ± 10 Ω
Cable Loss: 10 MHz 100 MHz	 < 0.6 dB < 2.0 dB	 n/a n/a	 1.8 dB 6 dB
Cable Length	5 m	7.62 m	7.62 m

Note: n/a – Not Available

APPENDIX H ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

This appendix defines alternate pin assignments for specific Quadrax contact positions on the J3 and J4 connectors. The following table identifies the affected contact positions:

Table H-1 – Contact Positions

Connector J3	Connector J4
	J4 – A
J3 – D	J4 – D
J3 – G	J4 – G
	J4 – K
	J4 – N
	J4 – S

This Appendix refers to the alternate pin allocations for connectors J3 and J4, as J3A and J4A respectively.

The J3 and J4 pin assignments listed in Section 4 and Appendix B of this specification do not support the best practices, defined in ARINC 664 Part 2, for terminating Quadrax contacts with Star Quad wire.

ARINC 664 Part 2 contains guidance for maintaining the geometric relationship of the Star Quad wire's color code lay with the pin assignments in the Quadrax contact. In addition, ARINC 664 Part 2 defines aircraft level end-to-end implementation guidelines for systems that use Quadrax contacts.

There is strong support by some aircraft manufacturers to maintain uniformity in Quadrax contact implementation and wiring practices, regardless of signal type used (Ethernet, RS-422, USB, LVDS, DVI, etc.). For that reason, some aircraft manufacturers will only support the J3A and J4A alternate pin definition.

Note: Some EFB installations may use twisted shielded pair wire, instead of Star Quad wire with Quadrax contacts. Rules and constraints for terminating twisted shielded pair wire, instead of Star Quad wire, to Quadrax contacts are not addressed in ARINC 664 Part 2.

Contained in this Appendix is:

- J3A Connector Description by Location of Socket
- J4A Connector Description by Location of Socket
- J3A Connector Description by Signal Function
- J4A Connector Description by Signal Function
- J3A Connector Termination Figure
- J4A Connector Termination Figure

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ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Table H-2 – J3A Connector Description by Location of Socket

Connector	Location	Abbrev	Description	Type
J3A	a	RS232_2_GND	RS-232 Return	22D
J3A	A-1	ETH 3_TX+	Ethernet Transmit +	Quadrax
J3A	A-2	ETH 3_RX+	Ethernet Receive +	Quadrax
J3A	A-3	ETH 3_TX-	Ethernet Transmit -	Quadrax
J3A	A-4	ETH 3_RX-	Ethernet Receive -	Quadrax
J3A	A-S	ETH 3_SH	Ethernet Shield	Quadrax
J3A	b	A717_2_RX+	ARINC 717 RX Data+	22D
J3A	B	A429_5_RX+	Printer to EFB (Receive +)	22D
J3A	C	A429_5_RX-	Printer to EFB (Receive -)	22D
J3A	c	A429_4_RXSH	ARINC 429 RX Shield	22D
J3A	d	A429_4_RX+	ARINC 429 Receiver +	22D
J3A	D-2	X_FP_D0+_TX	Cross LCD Flat Panel Data line 0 (R2-7,G2) TX	Quadrax
		X_TDMS_D0+_TX	Cross DVI Data Line 0_TX	
J3A	D-1	X_FP_D1+_TX	Cross LCD Flat Panel Data line 1 (G3-7,B2-3) TX	Quadrax
		X_TDMS_D1+_TX	Cross DVI Data Line 1_TX	
J3A	D-4	X_FP_D0-_TX	Cross LCD Flat Panel Data line 0 (R2-7,G2) TX	Quadrax
		X_TDMS_D0-_TX	Cross DVI Data Line 0_TX	
J3A	D-3	X_FP_D1-_TX	Cross LCD Flat Panel Data line 1 (G3-7,B2-3) TX	Quadrax
		X_TDMS_D1-_TX	Cross DVI Data Line 1_TX	
J3A	D-S	X_D1_SH	Shield	Quadrax
J3A	e	A429_3_RX+	ARINC 429 Receiver +	22D
J3A	E	A429_2_RX+	ARINC 429 Receiver +	22D
J3A	F	A429_2_RX-	ARINC 429 Receiver -	22D
J3A	f	A429_3_RX-	ARINC 429 Receiver -	22D
J3A	g	RS232_1_CTS	Clear To Send	22D
J3A	G-2	X_FP_D2+_TX	Cross LCD Flat Panel Data line 2 (B4-7,HSYNC,VSYNC,DE) TX	Quadrax
		X_TDMS_D2+_TX	Cross DVI Data Line 2_TX	
J3A	G-1	X_FP_CLK+_TX	Cross LCD Flat Panel Clock TX	Quadrax
		X_TDMS_CLK+_TX	Cross DVI Clock_TX	
J3A	G-4	X_FP_D2-_TX	Cross LCD Flat Panel Data line 2 (B4-7,HSYNC,VSYNC,DE) TX	Quadrax
		X_TDMS_D2-_TX	Cross DVI Data Line 2_TX	
J3A	G-3	X_FP_CLK-_TX	Cross LCD Flat Panel Clock TX	Quadrax
		X_TDMS_CLK-_TX	Cross DVI Clock_TX	
J3A	G-S	X_D2_SH	Shield	Quadrax
J3A	h	RS232_1_DTR	Data Terminal Ready	22D
J3A	H	A429_6_TX-	EFB to Printer (Transmitter -)	22D
J3A	J	A429_6_TX+	EFB to Printer (Transmitter +)	22D
J3A	k	RS232_1_DSR	Data Set Ready	22D
J3A	K-1	ETH 2_TX+	Ethernet Transmit +	Quadrax
		X_FP_D0+_RX	Cross LCD Flat Panel Data line 0 (R2-7,G2) RX	
		X_TDMS_D0+_RX	Cross DVI Data Line 0_RX	
J3A	K-2	ETH 2_RX+	Ethernet Receive +	Quadrax
		X_FP_D1+_RX	Cross LCD Flat Panel Data line 1 (G3-7,B2-3) RX	
		X_TDMS_D1+_RX	Cross DVI Data Line 1 RX	

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ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J3A	K-3	ETH 2_TX-	Ethernet Transmit -	Quadrax
		X_FP_D0-_RX	Cross LCD Flat Panel Data line 0 (R2-7,G2) RX	
		X_TDMS_D0-_RX	Cross DVI Data Line 0 RX	
J3A	K-4	ETH 2_RX-	Ethernet Receive -	Quadrax
		X_FP_D1-_RX	Cross LCD Flat Panel Data line 1 (G3-7,B2-3) RX	
		X_TDMS_D1-_RX	Cross DVI Data Line 1_RX	
J3A	K-S	ETH 2_SH	Ethernet Shield	Quadrax
J3A	L	A429_7_RTX-	ARINC 429 Receiver or Transmitter -	22D
J3A	M	A429_7_RTX+	ARINC 429 Receiver or Transmitter +	22D
J3A	m	RS232_1_DCD	Data Carrier Detect	22D
J3A	n	RS232_1_GND	RS-232 Return	22D
J3A	N-1	X_FP_D2+_RX	Cross LCD Flat Panel Data line 2 (B4-7,HSYNC,VSYNC,DE) RX	Quadrax
		X_TDMS_D2+_RX	Cross DVI Data Line 2_RX	
J3A	N-2	X_FP_CLK+_RX	Cross LCD Flat Panel Clock RX	Quadrax
		X_TDMS_CLK+_RX	Cross DVI Clock_RX	
J3A	N-3	X_FP_D2-RX	Cross LCD Flat Panel Data line 2 (B4-7,HSYNC,VSYNC,DE) RX	Quadrax
		X_TDMS_D2-_RX	Cross DVI Data Line 2_RX	
J3A	N-4	X_FP_CLK-_RX	Cross LCD Flat Panel Clock RX	Quadrax
		X_TDMS_CLK-_RX	Cross DVI Clock_RX	
J3A	N-S	X_NS_SH	Shield	Quadrax
J3A	p	RS232_1_TX	Transmit Data	22D
J3A	P	A429_8_RX-	ARINC 429 Receiver -	22D
J3A	q	A717_2_RXSH	ARINC 717 RX Shield	22D
J3A	r	A717_2_RX-	ARINC 717 RX Data-	22D
J3A	R	A429_8_RX+	ARINC 429 Receiver +	22D
J3A	s	A429_4_RX-	ARINC 429 Receiver -	22D
J3A	S-1	RS422_TXD+	Transmit Data +	Quadrax
J3A	S-2	RS422_RXD+	Receive Data +	Quadrax
J3A	S-3	RS422_TXD-	Transmit Data -	Quadrax
J3A	S-4	RS422_RXD-	Receive Data -	Quadrax
J3A	S-S	RS422_SH	RS422 Shield	Quadrax
J3A	t	A429_3_RXSH	ARINC 429 RX Shield	22D
J3A	T	RS232_2_TX	Transmit Data	22D
J3A	u	RS232_1_RI	Ring Indicator	22D
J3A	U	RS232_2_RX	Receive Data	22D
J3A	V	A429_5_RXSH	Printer to EFB (RX Shield)	22D
J3A	v	RS232_1_RTS	Ready To Send	22D
J3A	w	RS232_1_RX	Receive Data	22D
J3A	W	A429_2_RXSH	ARINC 429 RX Shield	22D
J3A	X	A429_6_TXSH	EFB to Printer (TX Shield)	22D
J3A	Y	A429_7_RTXSH	ARINC 429 RX/TX Shield	22D
J3A	Z	A429_8_RXSH	ARINC 429 RX Shield	22D

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Table H-3 – J4A Connector Description by Location of Socket

Connector	Location	Abbrev	Description	Type
J4A	a	DispDCPWR	Power from AID to display	22D
J4A	A-2	FP_D0+	LCD flat panel data line 0 (R2-7,G2)	Quadrax
		TMDS_D0+	DVI Data Line 0 NOTE: only single link supported	
J4A	A-1	FP_D1+	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
		TMDS_CLK+	DVI Clock	
J4A	A-4	FP_D0-	LCD flat panel data line 0 (R2-7,G2)	Quadrax
		TMDS_D0-	DVI Data Line 0	
J4A	A-3	FP_D1-	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
		TMDS_CLK-	DVI Clock	
J4A	A-S	AS_SH	Shield	Quadrax
J4A	B	Ground	Ground	22D
J4A	b	AC_DISC_5	Reserved for aircraft specific discrete	22D
J4A	C	Ground	Ground	22D
J4A	c	Ground	Ground	22D
J4A	d	AC_DISC_6	Reserved for aircraft specific discrete	22D
J4A	D-2	FP_D2+	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
		TMDS_D1+	DVI Data Line 1	
J4A	D-1	FP_D3+	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
		TMDS_D2+	DVI Data Line 2	
J4A	D-4	FP_D2-	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
		TMDS_D1-	DVI Data Line 1	
J4A	D-3	FP_D3-	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
		TMDS_D2-	DVI Data Line 2	
J4A	D-S	DS_SH	Shield	Quadrax
J4A	e	28Vdc_ANNUN+	28Vdc Annunciator bus	22D
J4A	E	DispDCRtn	Power from AID to display	22D
J4A	f	28Vdc_ANNUN-	28Vdc Annunciator bus	22D
J4A	F	DispDCRtn	Power from AID to display	22D
J4A	g	DISP_3	Reserved for display use	22D
J4A	G-2	FP_CLK+	LCD flat panel clock	Quadrax
		DDCCLK	DVI Display Bus Clock	
J4A	G-1	FP_D4+	Future LCD flat panel data 4	Quadrax
J4A	G-4	FP_CLK-	LCD flat panel clock	Quadrax
		DDCDATA	DVI Display Bus Data	
J4A	G-3	FP_D4-	Future LCD flat panel data 4	Quadrax
J4A	G-S	GS_SH	Shield	Quadrax
J4A	H	Ground	Ground	22D
J4A	h	DISP_6	Reserved for display use	22D
J4A	J	Ground	Ground	22D
J4A	k	DISP_5	Reserved for display use	22D
J4A	K-2	USB_2_PWR	USB +5V power (0.5A max)	Quadrax
		PS2_2_PWR	PS2 Device Power	
J4A	K-1	USB_2_D+	USB Data + {5m max length}	Quadrax

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
		APS2_2_GND	PS2 Device Ground	
J4A	K-4	USB_2_GND	USB Ground return	Quadrax
		PS2_2_CLK	PS2 Device Clock	
J4A	K-3	USB_2_D-	USB Data - {5m max length}	Quadrax
		PS2_2_DATA	PS2 Device Data	Quadrax
J4A	K-S	KS_SH	Shield	Quadrax
J4A	L	Ground	Ground	22D
J4A	M	Ground	Ground	22D
J4A	m	DISP_4	Reserved for display use	22D
J4A	n	AC_1	Reserved for aircraft specific use	22D
J4A	N-2	USB_3_PWR	USB +5V power (0.5A max)	Quadrax
		PS2_3_PWR	PS2 Device Power	
J4A	N-1	USB_3_D+	USB Data + {5m max length}	Quadrax
		PS2_3_GND	PS2 Device Ground	
J4A	N-4	USB_3_GND	USB Ground return	Quadrax
		PS2_3_CLK	PS2 Device Clock	
J4A	N-3	USB_3_D-	USB Data - {5m max length}	Quadrax
		PS2_3_DATA	PS2 Device Data	
J4A	N-S	NS_SH	Shield	Quadrax
J4A	P	Ground	Ground	22D
J4A	p	AC_1	Reserved for aircraft specific use	22D
J4A	q	AC_DISC_7	Reserved for aircraft specific discrete	22D
J4A	R	Ground	Ground	22D
J4A	r	AC_1	Reserved for aircraft specific use	22D
J4A	s	5Vac_ANNUN+	5Vac Annunciator bus	22D
J4A	S-2	USB_4_PWR	USB +5V power (0.5A max)	Quadrax
		PS2_4_PWR	PS2 Device Power	
J4A	S-1	USB_4_D+	USB Data + {5m max length}	Quadrax
		PS2_4_GND	PS2 Device Ground	
J4A	S-4	USB_4_GND	USB Ground return	Quadrax
		PS2_4_CLK	PS2 Device Clock	
J4A	S-3	USB_4_D-	USB Data - {5m max length}	Quadrax
		PS2_4_DATA	PS2 Device Data	
J4A	S-S	SS_SH	Shield	Quadrax
J4A	t	5Vac_ANNUN-	5Vac Annunciator bus	22D
J4A	T	DispDCPWR	Power from AID to display	22D
J4A	U	DispDCPWR	Power from AID to display	22D
J4A	u	DISP_2	Reserved for display use	22D
J4A	V	Ground	Ground	22D
J4A	v	DISP_1	Reserved for display use	22D
J4A	W	DispDCRtn	Power from AID to display	22D
J4A	w	AC_1	Reserved for aircraft specific use	22D
J4A	X	DISP_8	Reserved for display use	22D
J4A	Y	DISP_7	Reserved for display use	22D
J4A	Z	Ground	Ground	22D

Table H-4 – J3A Connector Description by Signal Function

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J3A		A429_2	Secondary avionics data	
J3A	E	A429_2_RX+	ARINC 429 Receiver +	22D
J3A	F	A429_2_RX-	ARINC 429 Receiver -	22D
J3A	W	A429_2_RXSH	ARINC 429 RX Shield	22D
J3A		A429_3	Secondary avionics data	
J3A	e	A429_3_RX+	ARINC 429 Receiver +	22D
J3A	f	A429_3_RX-	ARINC 429 Receiver -	22D
J3A	t	A429_3_RXSH	ARINC 429 RX Shield	22D
J3A		A429_4	Secondary avionics data	
J3A	d	A429_4_RX+	ARINC 429 Receiver +	22D
J3A	s	A429_4_RX-	ARINC 429 Receiver -	22D
J3A	c	A429_4_RXSH	ARINC 429 RX Shield	22D
J3A		A429_5	Printer to EFB	
J3A	B	A429_5_RX+	Printer to EFB (Receiver +)	22D
J3A	C	A429_5_RX-	Printer to EFB (Receiver -)	22D
J3A	V	A429_5_RXSH	Printer to EFB (RX Shield)	22D
J3A		A429_6	EFB to Printer	
J3A	J	A429_6_TX+	EFB to Printer (Transmitter +)	22D
J3A	H	A429_6_TX-	EFB to Printer (Transmitter -)	22D
J3A	X	A429_6_TXSH	EFB to Printer (TX Shield)	22D
J3A		A429_7	Custom	
J3A	M	A429_7_RTX+	ARINC 429 Receiver or Transmitter +	22D
J3A	L	A429_7_RTX-	ARINC 429 Receiver or Transmitter -	22D
J3A	Y	A429_7_RTXSH	ARINC 429 RX/TX Shield	22D
J3A		A429_8	Custom	
J3A	R	A429_8_RX+	ARINC 429 Receiver +	22D
J3A	P	A429_8_RX-	ARINC 429 Receiver -	22D
J3A	Z	A429_8_RXSH	ARINC 429 RX Shield	22D
J3A		ARINC 717	ARINC 717 FDR/QAR Data Bus	
J3A	b	A717_2_RX+	ARINC 717 RX Data+	22D
J3A	r	A717_2_RX-	ARINC 717 RX Data-	22D
J3A	q	A717_2_RXSH	ARINC 717 RX Shield	22D
J3A		Ethernet #2	Directly connected to Ethernet #2 of other Connector	
J3A	K-1	ETH 2_TX+	Ethernet Transmit +	Quadrax
J3A	K-3	ETH 2_TX-	Ethernet Transmit -	Quadrax
J3A	K-2	ETH 2_RX+	Ethernet Receive +	Quadrax
J3A	K-4	ETH 2_RX-	Ethernet Receive -	Quadrax
J3A	K-S	ETH 2_SH	Ethernet Shield	Quadrax
J3A		Ethernet #3	Aux (e.g., to display unit)	
J3A	A-1	ETH 3_TX+	Ethernet Transmit +	Quadrax
J3A	A-3	ETH 3_TX-	Ethernet Transmit -	Quadrax
J3A	A-2	ETH 3_RX+	Ethernet Receive +	Quadrax
J3A	A-4	ETH 3_RX-	Ethernet Receive -	Quadrax
J3A	A-S	ETH 3_SH	Ethernet Shield	Quadrax
J3A		RS-422	RS-422 full duplex interface	
J3A	S-2	RS422_RXD+	Receive Data +	Quadrax

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J3A	S-4	RS422_RXD-	Receive Data -	Quadrax
J3A	S-1	RS422_TXD+	Transmit Data +	Quadrax
J3A	S-3	RS422_TXD-	Transmit Data -	Quadrax
J3A	S-S	RS422_SH	RS422 Shield	Quadrax
J3A		RS232-2	send/receive only	
J3A	T	RS232_2_TX	Transmit Data	22D
J3A	U	RS232_2_RX	Receive Data	22D
J3A	a	RS232_2_GND	RS-232 Return	22D
J3A		RS232-1	including flow control	
J3A	p	RS232_1_TX	Transmit Data	22D
J3A	w	RS232_1_RX	Receive Data	22D
J3A	g	RS232_1_CTS	Clear To Send	22D
J3A	v	RS232_1_RTS	Ready To Send	22D
J3A	m	RS232_1_DCD	Data Carrier Detect	22D
J3A	k	RS232_1_DSR	Data Set Ready	22D
J3A	h	RS232_1_DTR	Data Terminal Ready	22D
J3A	u	RS232_1_RI	Ring Indicator	22D
J3A	n	RS232_1_GND	RS-232 Return	22D
J3A		Cross Video_RX	Cross Video Receive (LVDS or DVI)	
J3A	K-1	X_FP_D0+_RX	Cross LCD flat panel data line 0 (R2-7,G2) RX	Quadrax
J3A	K-3	X_FP_D0-_RX	Cross LCD flat panel data line 0 (R2-7,G2) RX	Quadrax
J3A	K-2	X_FP_D1+_RX	Cross LCD flat panel data line 1 (G3-7,B2-3) RX	Quadrax
J3A	K-4	X_FP_D1-_RX	Cross LCD flat panel data line 1 (G3-7,B2-3) RX	Quadrax
J3A	K-S	X_D1_SH	Shield	Quadrax
J3A	N-1	X_FP_D2+_RX	Cross LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE) RX	Quadrax
J3A	N-3	X_FP_D2-_RX	Cross LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE) RX	Quadrax
J3A	N-2	X_FP_CLK+_RX	Cross LCD flat panel Clock RX	Quadrax
J3A	N-4	X_FP_CLK-_RX	Cross LCD flat panel Clock RX	Quadrax
J3A	N-S	X_D2_SH	Shield	Quadrax
J3A	K-1	X_TDMS_D0+_RX	Cross DVI Data Line 0_RX	Quadrax
J3A	K-3	X_TDMS_D0-_RX	Cross DVI Data Line 0_RX	Quadrax
J3A	K-2	X_TDMS_D1+_RX	Cross DVI Data Line 1_RX	Quadrax
J3A	K-4	X_TDMS_D1-_RX	Cross DVI Data Line 1_RX	Quadrax
J3A	K-S	X_D1_SH	Shield	Quadrax
J3A	N-1	X_TDMS_D2+_RX	Cross DVI Data Line 2_RX	Quadrax
J3A	N-3	X_TDMS_D2-_RX	Cross DVI Data Line 2_RX	Quadrax
J3A	N-2	X_TDMS_CLK+_RX	Cross DVI Clock_RX	Quadrax
J3A	N-4	X_TDMS_CLK-_RX	Cross DVI Clock_RX	Quadrax
J3A	N-S	X_D2_SH	Shield	Quadrax
J3A		Cross_Video TX	Cross Video Transmit (LVDS or DVI)	
J3A	D-2	X_FP_D0+_TX	Cross LCD Flat Panel Data Line 0 (R2-7,G2) TX	Quadrax
J3A	D-4	X_FP_D0-_TX	Cross LCD Flat Panel Data Line 0 (R2-7,G2) TX	Quadrax

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J3A	D-1	X_FP_D1+_TX	Cross LCD Flat Panel Data Line 1 (G3-7,B2-3) TX	Quadrax
J3A	D-3	X_FP_D1-_TX	Cross LCD Flat Panel Data Line 1 (G3-7,B2-3) TX	Quadrax
J3A	D-S	X_D1_SH	Shield	Quadrax
J3A	G-2	X_FP_D2+_TX	Cross LCD Flat Panel Data Line 2 (B4-7,HSYNC,VSYNC,DE) TX	Quadrax
J3A	G-4	X_FP_D2-_TX	Cross LCD Flat Panel Data Line 2 (B4-7,HSYNC,VSYNC,DE) TX	Quadrax
J3A	G-1	X_FP_CLK+_TX	Cross LCD Flat Panel Clock TX	Quadrax
J3A	G-3	X_FP_CLK-_TX	Cross LCD Flat Panel Clock TX	Quadrax
J3A	G-S	X_D2_SH	Shield	Quadrax
J3A	D-2	X_TDMS_D0+_TX	Cross DVI Data Line 0_TX	Quadrax
J3A	D-4	X_TDMS_D0-_TX	Cross DVI Data Line 0_TX	Quadrax
J3A	D-1	X_TDMS_D1+_TX	Cross DVI Data Line 1_TX	Quadrax
J3A	D-3	X_TDMS_D1-_TX	Cross DVI Data Line 1_TX	Quadrax
J3A	D-S	X_D1_SH	Shield	Quadrax
J3A	G-2	X_TDMS_D2+_TX	Cross DVI Data Line 2_TX	Quadrax
J3A	G-4	X_TDMS_D2-_TX	Cross DVI Data Line 2_TX	Quadrax
J3A	G-1	X_TDMS_CLK+_TX	Cross DVI Clock_TX	Quadrax
J3A	G-3	X_TDMS_CLK-_TX	Cross DVI Clock_TX	Quadrax
J3A	G-S	X_D2_SH	Shield	Quadrax

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Table H-5 – J4A Connector Description by Signal Function

Connector	Location	Abbrev	Description	Type
J4A		Video	DVI or LVDS = 5 twisted pairs = 10 wires	
J4A	A-2	FP_D0+	LCD flat panel data line 0 (R2-7,G2)	Quadrax
J4A	A-4	FP_D0-	LCD flat panel data line 0 (R2-7,G2)	Quadrax
J4A	A-1	FP_D1+	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
J4A	A-3	FP_D1-	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
J4A	A-S	AS_SH	Shield	Quadrax
J4A	D-2	FP_D2+	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
J4A	D-4	FP_D2-	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
J4A	D-1	FP_D3+	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
J4A	D-3	FP_D3-	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
J4A	D-S	DS_SH	Shield	Quadrax
J4A	G-2	FP_CLK+	LCD flat panel clock	Quadrax
J4A	G-4	FP_CLK-	LCD flat panel clock	Quadrax
J4A	G-1	FP_D4+	Future LCD flat panel data 4	Quadrax
J4A	G-3	FP_D4-	Future LCD flat panel data 4	Quadrax
J4A	G-S	GS_SH	Shield	Quadrax
J4A	A-2	TMDS_D0+	DVI Data Line 0 NOTE: only single link supported	Quadrax
J4A	A-4	TMDS_D0-	DVI Data Line 0	Quadrax
J4A	D-2	TMDS_D1+	DVI Data Line 1	Quadrax
J4A	D-4	TMDS_D1-	DVI Data Line 1	Quadrax
J4A	D-1	TMDS_D2+	DVI Data Line 2	Quadrax
J4A	D-3	TMDS_D2-	DVI Data Line 2	Quadrax
J4A	D-S	DS_SH	Shield	Quadrax
J4A	A-1	TMDS_CLK+	DVI Clock	Quadrax
J4A	A-3	TMDS_CLK-	DVI Clock	Quadrax
J4A	A-S	AS_SH	Shield	Quadrax
J4A	G-2	DDCCLK	DVI Display Bus Clock	Quadrax
J4A	G-4	DDCDATA	DVI Display Bus Data	Quadrax
J4A		USB_2/PS2_2	Secondary USB device or PS/2	
J4A	K-2	USB_2_PWR	USB +5V power (0.5A max)	Quadrax
J4A	K-1	USB_2_D+	USB Data + {5m max length}	Quadrax
J4A	K-3	USB_2_D-	USB Data - {5m max length}	Quadrax
J4A	K-4	USB_2_GND	USB Ground return	Quadrax
J4A	K-S	KS_SH	Shield	Quadrax
J4A	K-4	PS2_2_CLK	PS2 Device Clock	Quadrax
J4A	K-3	PS2_2_DATA	PS2 Device Data	Quadrax
J4A	K-2	PS2_2_PWR	PS2 Device Power	Quadrax
J4A	K-1	PS2_2_GND	PS2 Device Ground	Quadrax
J4A	K-S	KS_SH	Shield	Quadrax
J4A		USB_3/PS2_3	Secondary USB device or PS/2	
J4A	N-2	USB_3_PWR	USB +5V power (0.5A max)	Quadrax

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J4A	N-1	USB_3_D+	USB Data + {5m max length}	Quadrax
J4A	N-3	USB_3_D-	USB Data - {5m max length}	Quadrax
J4A	N-4	USB_3_GND	USB Ground return	Quadrax
J4A	N-S	NS_SH	USB Shield	Quadrax
J4A	N-4	PS2_3_CLK	PS2 Device Clock	Quadrax
J4A	N-3	PS2_3_DATA	PS2 Device Data	Quadrax
J4A	N-2	PS2_3_PWR	PS2 Device Power	Quadrax
J4A	N-1	PS2_3_GND	PS2 Device Ground	Quadrax
J4A	N-S	NS_SH	PS2 Shield	Quadrax
J4A		USB_4/PS2_4	Secondary USB device or PS/2	
J4A	S-2	USB_4_PWR	USB +5V power (0.5A max)	Quadrax
J4A	S-1	USB_4_D+	USB Data + {5m max length}	Quadrax
J4A	S-3	USB_4_D-	USB Data - {5m max length}	Quadrax
J4A	S-4	USB_4_GND	USB Ground return	Quadrax
J4A	S-S	SS_SH	USB Shield	Quadrax
J4A	S-4	PS2_4_CLK	PS2 Device Clock	Quadrax
J4A	S-3	PS2_4_DATA	PS2 Device Data	Quadrax
J4A	S-2	PS2_4_PWR	PS2 Device Power	Quadrax
J4A	S-1	PS2_4_GND	PS2 Device Ground	Quadrax
J4A	S-S	SS_SH	PS2 Shield	Quadrax
J4A		Reserved	Reserved for aircraft specific discrete	
J4A	B	AC_DISC_5	Reserved for aircraft specific discrete	22D
J4A	D	AC_DISC_6	Reserved for aircraft specific discrete	22D
J4A	q	AC_DISC_7	Reserved for aircraft specific discrete	22D
J4A		Reserved	Reserved for aircraft specific use	
J4A	r	AC_1	Reserved for aircraft specific use	22D
J4A	p	AC_1	Reserved for aircraft specific use	22D
J4A	w	AC_1	Reserved for aircraft specific use	22D
J4A	n	AC_1	Reserved for aircraft specific use	22D
J4A		EFB Lighting	Display lighting, bezel keys lighting, dimming	
J4A	e	28Vdc_ANNUN+	28Vdc Annunciator bus	22D
J4A	f	28Vdc_ANNUN-	28Vdc Annunciator bus	22D
J4A	s	5Vac_ANNUN+	5Vac Annunciator bus	22D
J4A	t	5Vac_ANNUN-	5Vac Annunciator bus	22D
J4A		DC Power Return	Power from AID to display	
J4A	U	DispDCPWR	Power from AID to display	22D
J4A	T	DispDCPWR	Power from AID to display	22D
J4A	a	DispDCPWR	Power from AID to display	22D
J4A	W	DispDCRtn	Power from AID to display	22D
J4A	E	DispDCRtn	Power from AID to display	22D
J4A	F	DispDCRtn	Power from AID to display	22D
J4		Ground pins	Ground Pins	
J4	B	Ground	Ground	22D
J4	V	Ground	Ground	22D
J4	C	Ground	Ground	22D
J4	J	Ground	Ground	22D

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

Connector	Location	Abbrev	Description	Type
J4A	H	Ground	Ground	22D
J4A	c	Ground	Ground	22D
J4A	M	Ground	Ground	22D
J4A	L	Ground	Ground	22D
J4A	P	Ground	Ground	22D
J4A	R	Ground	Ground	22D
J4A	Z	Ground	Ground	22D
J4A		Reserved	Reserved for display use	
J4A	v	DISP_1	Reserved for display use	22D
J4A	u	DISP_2	Reserved for display use	22D
J4A	g	DISP_3	Reserved for display use	22D
J4A	m	DISP_4	Reserved for display use	22D
J4A	k	DISP_5	Reserved for display use	22D
J4A	h	DISP_6	Reserved for display use	22D
J4A	Y	DISP_7	Reserved for display use	22D
J4A	X	DISP_8	Reserved for display use	22D

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

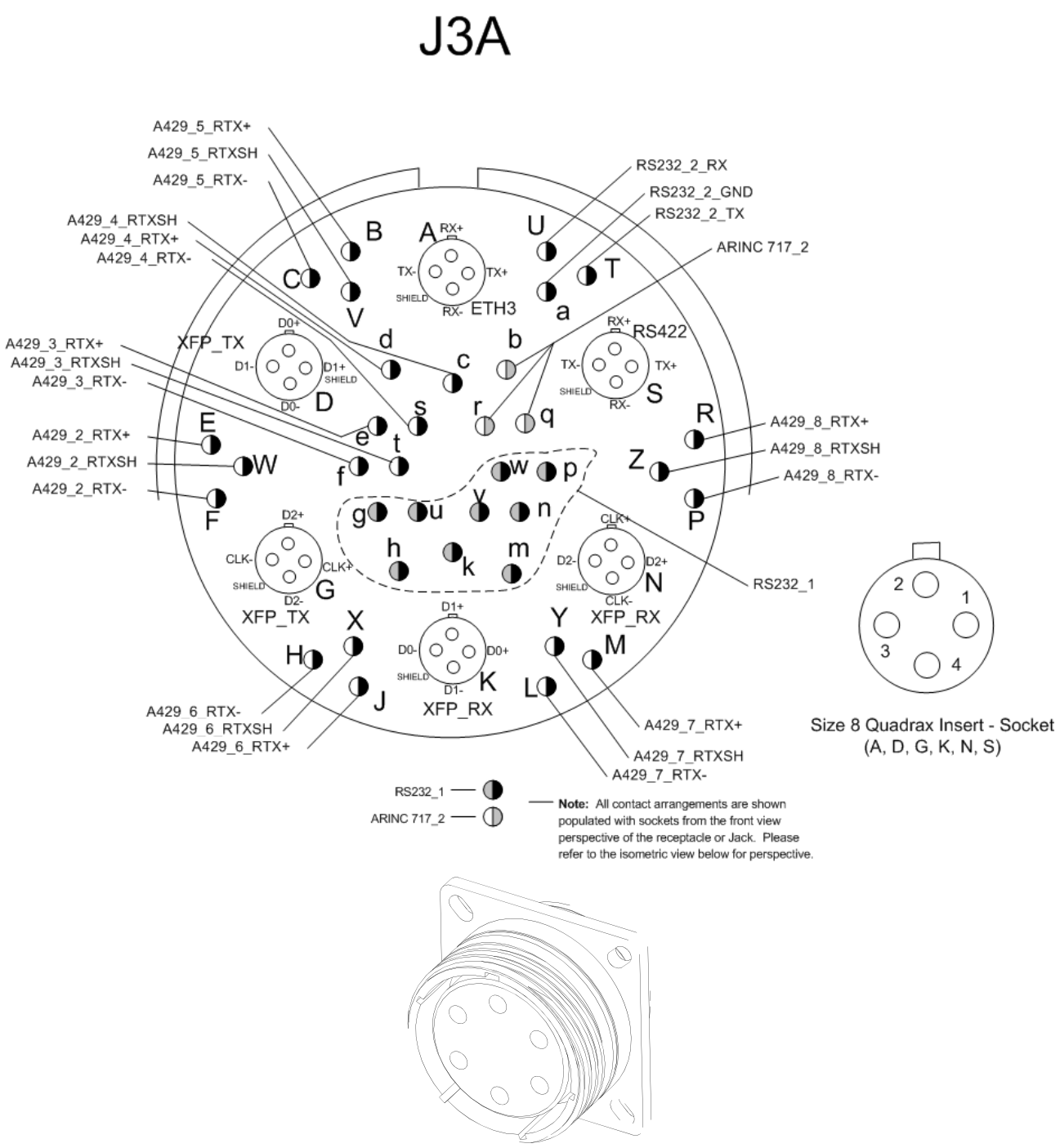


Figure H-1 – J3: EN3645-F0JL17FB

APPENDIX H
ALTERNATE J3A AND J4A CONNECTORS AND PIN REQUIREMENTS

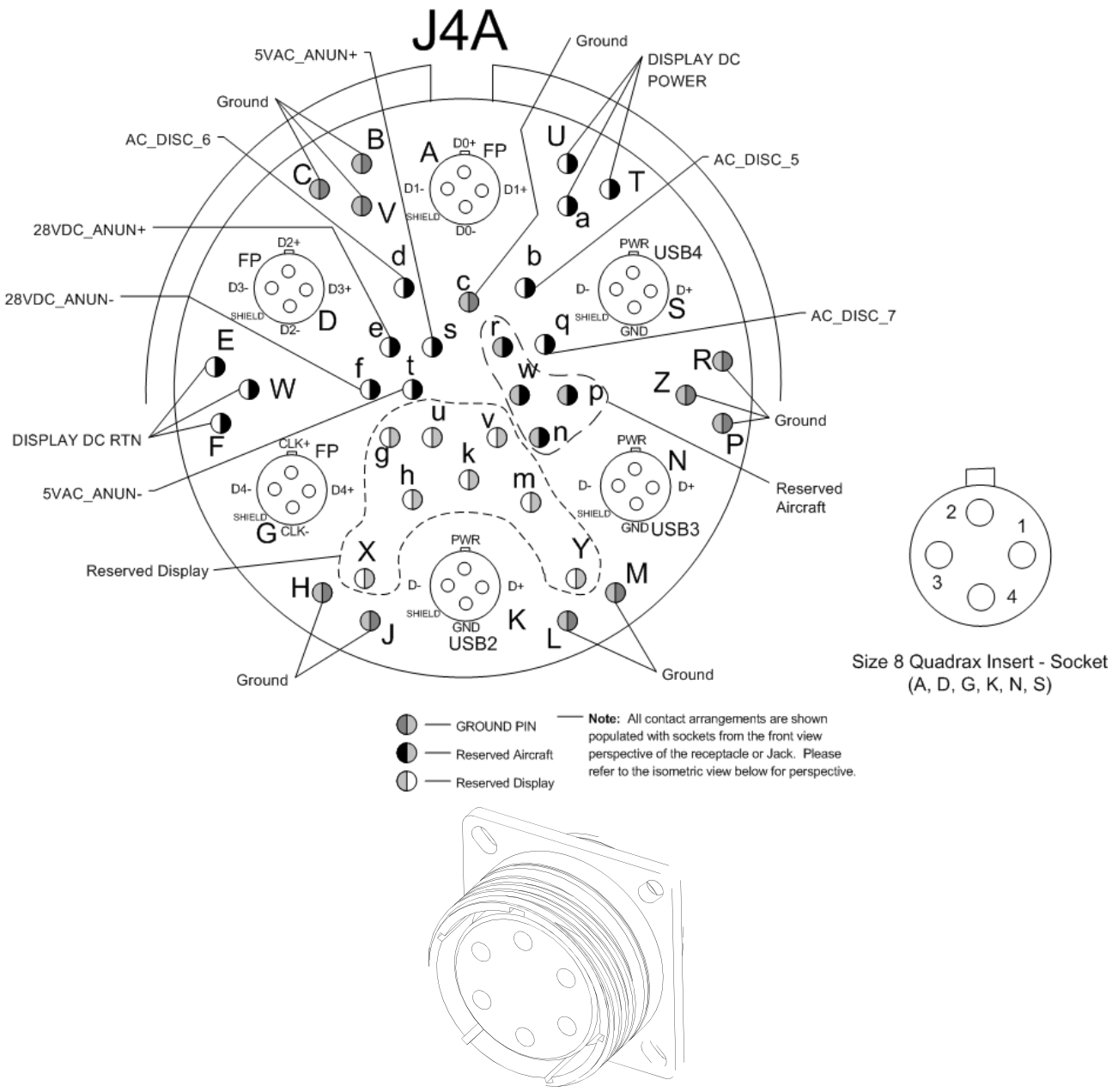


Figure H-2 – J4: EN3645-F0JL17FC

APPENDIX I METHODS FOR TERMINATING TWISTED-SHIELDED PAIR CABLE INTO QUADRAX CONTACTS

I-1 Introduction

Appendix I provides general information and guidance for the termination of Twisted Shielded Pair LVDS type wire into Quadrax contacts. Since the information and instructions are generic, minor adjustments may be required for specific contacts. The assembler should contact the connector and cable manufacture for specific information for a given set of components.

I-2 Termination Workmanship

Termination of differential pairs of any wire type to a Quadrax insert requires careful attention to factors that may impact electrical and mechanical performance, particularly on high-speed signaling such as LVDS. To provide for the best possible performance the following factors should be considered:

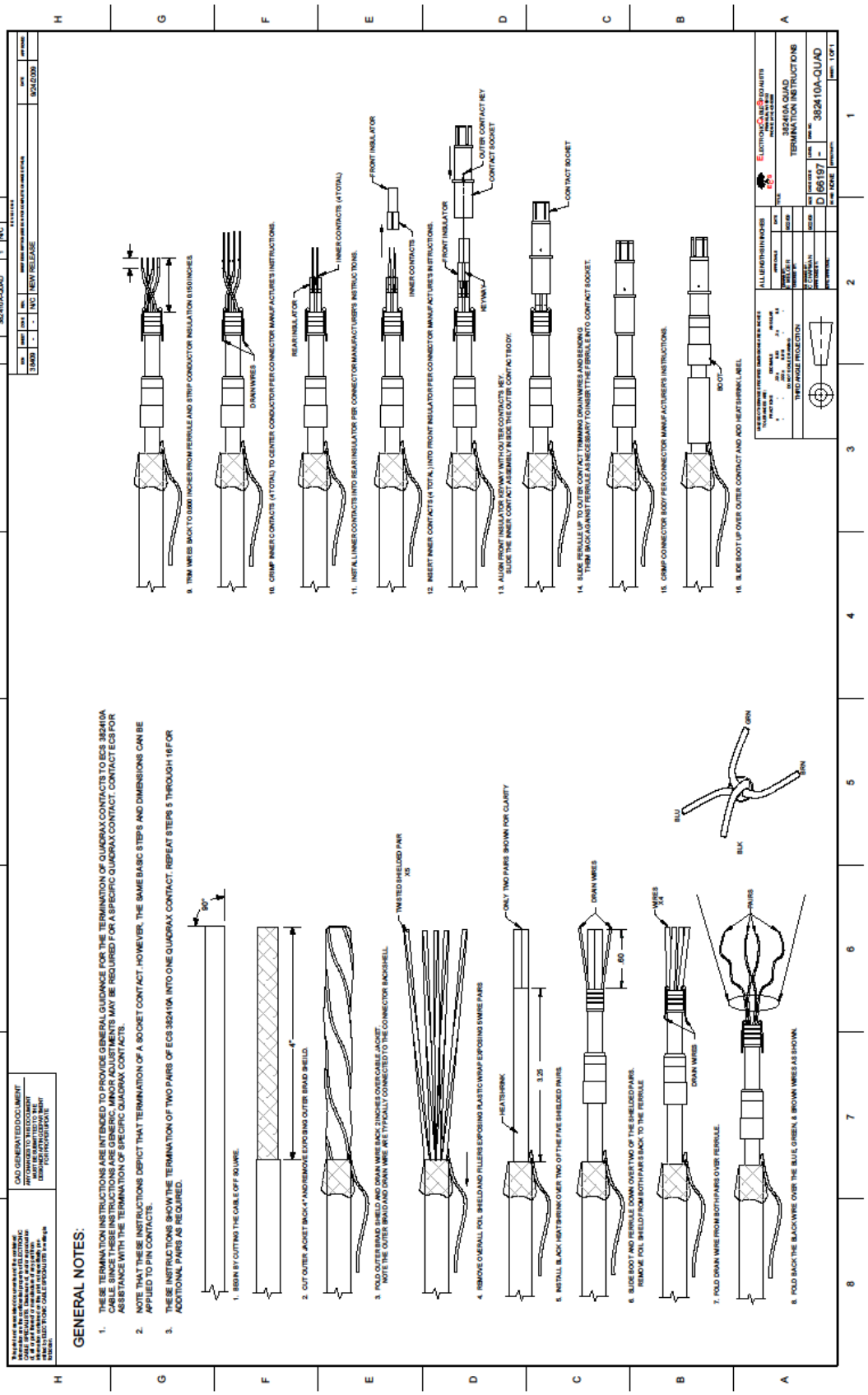
Differential Impedance Control – Termination impedance must be as close as possible to the characteristic impedance of the cable. Untwisting and separating the wires should be kept to a minimum as it can lead to an inductive loop and high impedance discontinuity which causes signal reflections. Impedance-controlled termination can be verified using TDR.

Return Path Continuity – Wire shields or drain wires must be terminated to the Quadrax shield for a continuous return path from signal driver to receiver. A break in the shielding will induce signal reflections and may present EMI issues. In the case of star quad cabling, there is one shield around four wires that must be terminated to one Quadrax contact. In the case of TSP, there are two shields – one around each pair – that must be terminated to one Quadrax contact. Additionally, if the TSP has an overall shield it should be terminated to the connector backshell.

Propagation Delay Skew Control – When trimming the wires for termination, the two wires of a differential pair are trimmed as close as possible to the same length. Also, for signaling over multiple parallel data lines such as LVDS, the wire pairs or quads must all be trimmed as close as possible to the same length with respect to each other for data/clock timing accuracy. Delay skew can also be quantified using TDR.

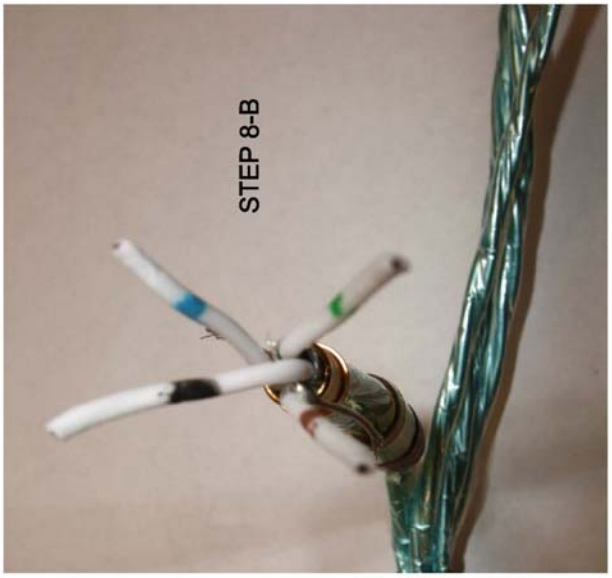
Mechanical Robustness – When specifying a connector part number, the Quadrax inserts must be appropriate for the wire gauge being used. Strain relief must be provided so that no wires or shields separate from their terminations.

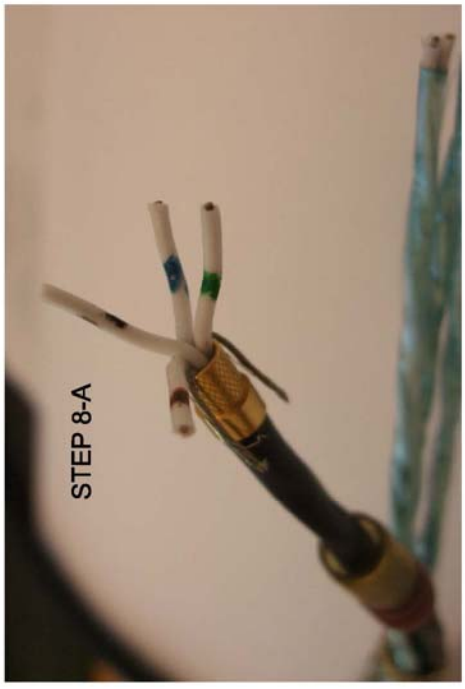
APPENDIX I
METHODS FOR TERMINATING TWISTED SHIELDED PAIR CABLE INTO QUADRAX CONTACTS



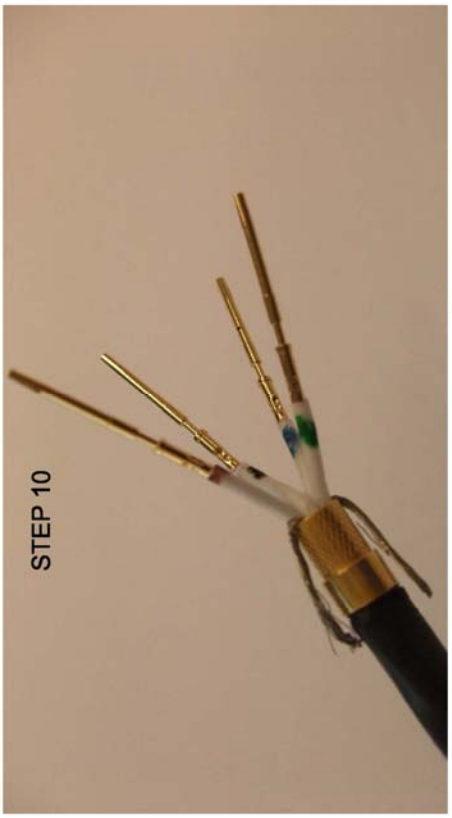
APPENDIX I
METHODS FOR TERMINATING TWISTED SHIELDED PAIR CABLE INTO QUADRAX CONTACTS

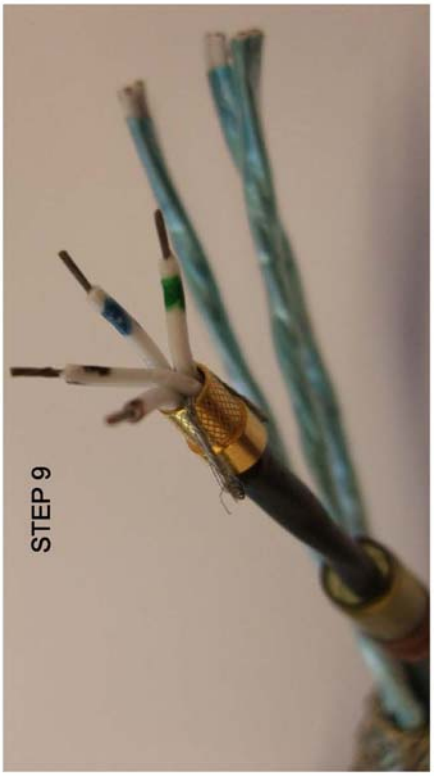
APPENDIX I
METHODS FOR TERMINATING TWISTED SHIELDED PAIR CABLE INTO QUADRAX CONTACTS





APPENDIX I
METHODS FOR TERMINATING TWISTED SHIELDED PAIR CABLE INTO QUADRAX CONTACTS





APPENDIX I
METHODS FOR TERMINATING TWISTED SHIELDED PAIR CABLE INTO QUADRAX CONTACTS

APPENDIX J EXAMPLE ENVIRONMENTAL TESTS FOR EFB EQUIPMENT

The following is a set of typical EFB environmental tests that should be considered by the EFB designer and the EFB system integrator. The actual RTCA DO-160/EUROCAE ED-14 environmental and EMI requirements for an EFB system may be specified by the aircraft system integrator. These tests are dependent on several factors of the system configuration, including:

- Installation location – Avionics bay or flight deck, window mount or cabinet location.
- Equipment classification – A Class 1 laptop may have different requirement levels than Class 2 or Class 3 installed equipment.
- Approval basis – Certified avionics equipment may have higher requirements than an operationally approved Portable Electronic Device (PED).
- Intended function – Performance characteristics must be sufficient for the environment.
- Input power – DC or AC power, constant or variable frequency, essential or non-essential bus.
- Data bus connectivity, e.g., ARINC 429, ARINC 818

Table J-1 – EFB Environmental Tests

RTCA DO-160E Section	TEST/EQUIPMENT	AID	EFB Terminal
		Cat/Remarks	Cat/Remarks
4.0	Temperature & Altitude	A1	A1
5.0	Temperature Variation	C	C
6.0	Humidity	A	A
7.0	Shock	B	B
8.0	Vibration (Random)	Cat S, Curve B	Cat S, Curve B
10.0	Water Proofness	W	W
15.0	Magnetic Effect	A	A
16.0	Power Input	A(WF)	A(WF)
17.0	Voltage Spike	A	A
18.0	AF Conducted Susceptibility	R(CF)	R(CF)
19.0	Induced Signal Susceptibility	Z(W)	Z(W)
20.0	RF Susceptibility	T	T
21.0	Emission of RF Energy	M	M
22.0	Lightning Induced Transient Susceptibility	A3J33	A3J33
25.0	Electrostatic Discharge (ESD)	A	A

APPENDIX K J5-1 AND J5-2 ALTERNATE TERMINAL CONNECTORS

Connectors J5-1 and J5-2 are intended as a smaller alternative terminal connector for J4. By removing signals and splitting the remaining signals into two smaller connectors, mechanical installation can be easier.

The references of these two connectors are:

J5-1: EN3645-F0GL75BN

J5-2: EN3646-RS01626BN

APPENDIX K
J5-1 AND J5-2 ALTERNATE TERMINAL CONNECTORS

Table K-1 – J5-1 Connector Description by Location of Socket

Connector	Location	Abbrev	Description	Type
J5-1	A-2	FP_D0+	LCD flat panel data line 0 (R2-7,G2)	Quadrax
		TMDS_D0+	DVI Data Line 0 NOTE: only single link supported	
J5-1	A-1	FP_D1+	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
		TMDS_CLK+	DVI Clock	
J5-1	A-4	FP_D0-	LCD flat panel data line 0 (R2-7,G2)	Quadrax
		TMDS_D0-	DVI Data Line 0	
J5-1	A-3	FP_D1-	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
		TMDS_CLK-	DVI Clock	
J5-1	A-S	AS_SH	Shield	Quadrax
J5-1	B-2	FP_D2+	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
		TMDS_D1+	DVI Data Line 1	
J5-1	B-1	FP_D3+	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
		TMDS_D2+	DVI Data Line 2	
J5-1	B-4	FP_D2-	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
		TMDS_D1-	DVI Data Line 1	
J5-1	B-3	FP_D3-	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
		TMDS_D2-	DVI Data Line 2	
J5-1	B-S	BS_SH	Shield	Quadrax
J5-1	D-2	FP_CLK+	SPARE: LCD flat panel clock	Quadrax
		DDCCLK	SPARE: DVI Display Bus Clock	
J5-1	D-1	FP_D4+	SPARE: Future LCD flat panel data 4	Quadrax
J5-1	D-4	FP_CLK-	SPARE: LCD flat panel clock	Quadrax
		DDCDATA	SPARE: DVI Display Bus Data	
J5-1	D-3	FP_D4-	SPARE: Future LCD flat panel data 4	Quadrax
J5-1	D-S	DS_SH	SPARE: Shield	Quadrax
J5-1	C-2	USB_2_PWR	USB +5V power (0.5A max)	Quadrax
		PS2_2_PWR	PS2 Device Power	
J5-1	C-1	USB_2_D+	USB Data + {5m max length}	Quadrax
		PS2_2_GND	PS2 Device Ground	
J5-1	C-4	USB_2_GND	USB Ground return	Quadrax
		PS2_2_CLK	PS2 Device Clock	
J5-1	C-3	USB_2_D-	USB Data - {5m max length}	Quadrax
		PS2_2_DATA	PS2 Device Data	Quadrax
J5-1	C-S	CS_SH	Shield	Quadrax

APPENDIX K
J5-1 AND J5-2 ALTERNATE TERMINAL CONNECTORS

Table K-2 – J5-2 Connector Description by Location of Socket

Connector	Location	Abbrev	Description	Type
J5-2	b	DispDCPWR	Power from AID to display	20
J5-2	a	DispDCPWR	Power from AID to display	20
J5-2	c	DispDCRtn	Power from AID to display	20
J5-2	Y	DispDCRtn	Power from AID to display	20
J5-2	H	DISP_1	Reserved for display use	20
J5-2	J	DISP_2	Reserved for display use	20
J5-2	K	DISP_6	Reserved for display use	20
J5-2	L	DISP_7	Reserved for display use	20
J5-2	M	Ground	Ground	20
J5-2	P	Ground	Ground	20
J5-2	X	Ground	Ground	20
J5-2	U	Ground	Ground	20
J5-2	F	Ground	Ground	20
J5-2	A	LP 5Vac_ANNUN+	LP 5Vac Annunciator bus	20
J5-2	S	LP 5Vac_ANNUN-	LP 5Vac Annunciator bus	20
J5-2	T	LP Shield	LP Shield	20
J5-2	D	LF 5Vac_ANNUN+	LF 5Vac Annunciator bus	20
J5-2	E	LF 5Vac_ANNUN-	LF 5Vac Annunciator bus	20
J5-2	V	LF Shield	LF Shield	20
J5-2	G	Light Test	DISP LP	20
J5-2	B	SPARE	SPARE	20
J5-2	C	SPARE	SPARE	20
J5-2	N	SPARE	SPARE	20
J5-2	R	SPARE	SPARE	20
J5-2	W	SPARE	SPARE	20
J5-2	Z	SPARE	SPARE	20

APPENDIX K
J5-1 AND J5-2 ALTERNATE TERMINAL CONNECTORS

Table K-3 – J5-1 Connector Description by Signal Function

Connector	Location	Abbrev	Description	Type
J5-1		Video	DVI or LVDS = 5 twisted pairs = 10 wires	
J5-1	A-2	FP_D0+	LCD flat panel data line 0 (R2-7,G2)	Quadrax
J5-1	A-4	FP_D0-	LCD flat panel data line 0 (R2-7,G2)	Quadrax
J5-1	A-1	FP_D1+	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
J5-1	A-3	FP_D1-	LCD flat panel data line 1 (G3-7,B2-3)	Quadrax
J5-1	A-S	AS_SH	Shield	Quadrax
J5-1	B-2	FP_D2+	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
J5-1	B-4	FP_D2-	LCD flat panel data line 2 (B4-7,HSYNC,VSYNC,DE)	Quadrax
J5-1	B-1	FP_D3+	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
J5-1	B-3	FP_D3-	LCD flat panel data line 3 (R0-1,G0-1,B0-1) 24 bit panel only	Quadrax
J5-1	B-S	BS_SH	Shield	Quadrax
J5-1	D-2	FP_CLK+	SPARE: LCD flat panel clock	Quadrax
J5-1	D-4	FP_CLK-	SPARE: LCD flat panel clock	Quadrax
J5-1	D-1	FP_D4+	SPARE: Future LCD flat panel data 4	Quadrax
J5-1	D-3	FP_D4-	SPARE: Future LCD flat panel data 4	Quadrax
J5-1	D-S	DS_SH	SPARE: Shield	Quadrax
J5-1	A-2	TMDS_D0+	DVI Data Line 0 NOTE: only single link supported	Quadrax
J5-1	A-4	TMDS_D0-	DVI Data Line 0	Quadrax
J5-1	B-2	TMDS_D1+	DVI Data Line 1	Quadrax
J5-1	B-4	TMDS_D1-	DVI Data Line 1	Quadrax
J5-1	B-1	TMDS_D2+	DVI Data Line 2	Quadrax
J5-1	B-3	TMDS_D2-	DVI Data Line 2	Quadrax
J5-1	B-S	BS_SH	Shield	Quadrax
J5-1	A-1	TMDS_CLK+	DVI Clock	Quadrax
J5-1	A-3	TMDS_CLK-	DVI Clock	Quadrax
J5-1	A-S	AS_SH	Shield	Quadrax
J5-1	D-2	DDCCLK	SPARE: DVI Display Bus Clock	Quadrax
J5-1	D-4	DDCDATA	SPARE: DVI Display Bus Data	Quadrax
J5-1		USB_2/PS2_2	Secondary USB device or PS/2	
J5-1	C-2	USB_2_PWR	USB +5V power (0.5A max)	Quadrax
J5-1	C-1	USB_2_D+	USB Data + {5m max length}	Quadrax
J5-1	C-3	USB_2_D-	USB Data - {5m max length}	Quadrax
J5-1	C-4	USB_2_GND	USB Ground return	Quadrax
J5-1	C-S	CS_SH	Shield	Quadrax
J5-1	C-4	PS2_2_CLK	PS2 Device Clock	Quadrax
J5-1	C-3	PS2_2_DATA	PS2 Device Data	Quadrax
J5-1	C-2	PS2_2_PWR	PS2 Device Power	Quadrax
J5-1	C-1	PS2_2_GND	PS2 Device Ground	Quadrax
J5-1	C-S	CS_SH	Shield	Quadrax

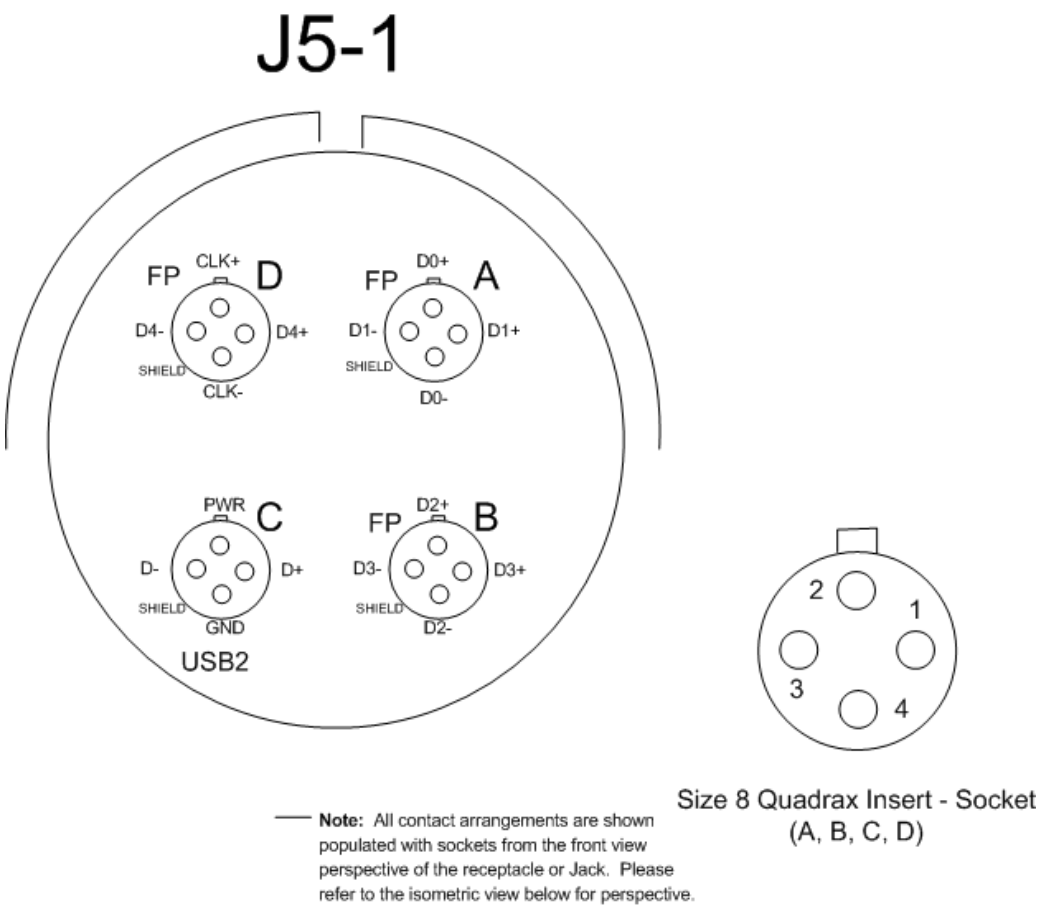
APPENDIX K
J5-1 AND J5-2 ALTERNATE TERMINAL CONNECTORS

Table K-4 – J5-2 Connector Description by Signal Function

Connector	Location	Abbrev	Description	Type
J5-2		DC Power Return	Power from AID to display	
J5-2	b	DispDCPWR	Power from AID to display	20
J5-2	a	DispDCPWR	Power from AID to display	20
J5-2	c	DispDCRtn	Power from AID to display	20
J5-2	Y	DispDCRtn	Power from AID to display	20
J5-2		Reserved	Reserved for display use	
J5-2	H	DISP_1	Reserved for display use	20
J5-2	J	DISP_2	Reserved for display use	20
J5-2	K	DISP_6	Reserved for display use	20
J5-2	L	DISP_7	Reserved for display use	20
J5-2		Ground pins	Ground Pins	
J5-2	M	Ground	Ground	20
J5-2	P	Ground	Ground	20
J5-2	X	Ground	Ground	20
J5-2	U	Ground	Ground	20
J5-2	F	Ground	Ground	20
J5-2		EFB Lighting	Display lighting, bezel keys lighting, dimming	
J5-2	A	LP 5Vac_ANNUN+	LP 5Vac Annunciator bus	20
J5-2	S	LP 5Vac_ANNUN-	LP 5Vac Annunciator bus	20
J5-2	T	LP Shield	LP Shield	20
J5-2	D	LF 5Vac_ANNUN+	LF 5Vac Annunciator bus	20
J5-2	E	LF 5Vac_ANNUN-	LF 5Vac Annunciator bus	20
J5-2	V	LF Shield	LF Shield	20
J5-2	G	Light Test	DISP LP	20
		SPARE	SPARE	
J5-2	B	SPARE	SPARE	20
J5-2	C	SPARE	SPARE	20
J5-2	N	SPARE	SPARE	20
J5-2	R	SPARE	SPARE	20
J5-2	W	SPARE	SPARE	20
J5-2	Z	SPARE	SPARE	20

APPENDIX K
J5-1 AND J5-2 ALTERNATE TERMINAL CONNECTORS

CONNECTOR TERMINATION



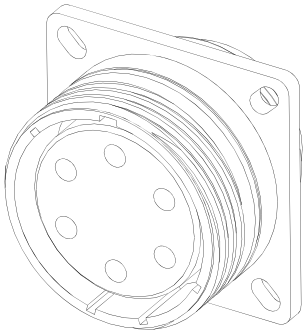


Figure K-1 – J5-1: EN3645-F0GL75BN

APPENDIX K
J5-1 AND J5-2 ALTERNATE TERMINAL CONNECTORS

CONNECTOR TERMINATION

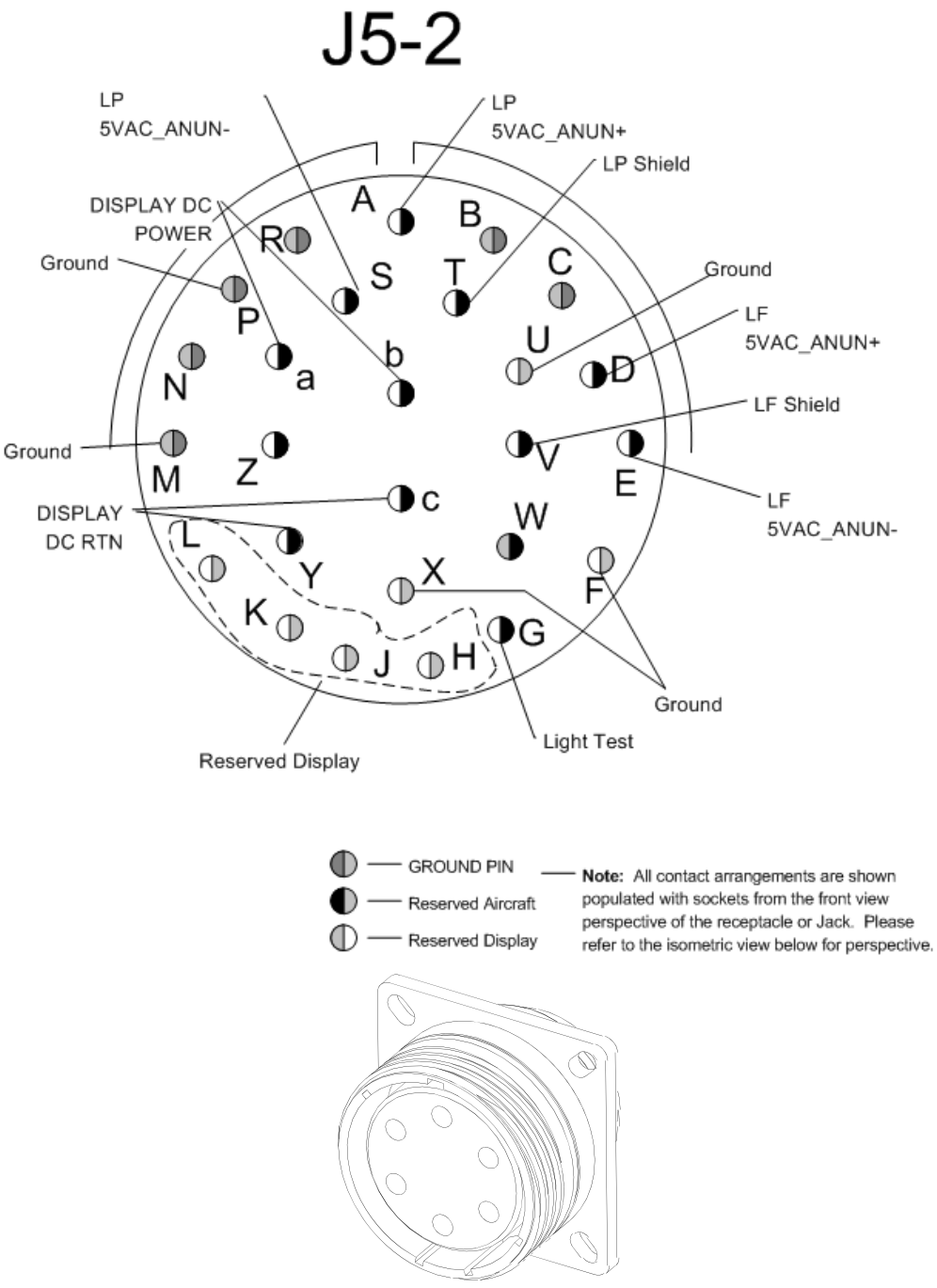


Figure K-2 – J5-2: EN3646-RS01626BN

APPENDIX L RFB TERMINAL INTERFACE

This appendix defines how an EFB (Electronic Flight Bag) PU (Processing Unit) can be accessed from a remote terminal.

This standard assumes IP (Internet Protocol) connectivity is provided between the EFB PU and the terminal. No other communication channels are required by this standard.

This appendix specifies connectors and physical communication channels between EFB PUs and Terminals. This appendix defines a higher level, concentrating on the actual data flow on these channels, or more precisely, on one specific channel kind – Ethernet.

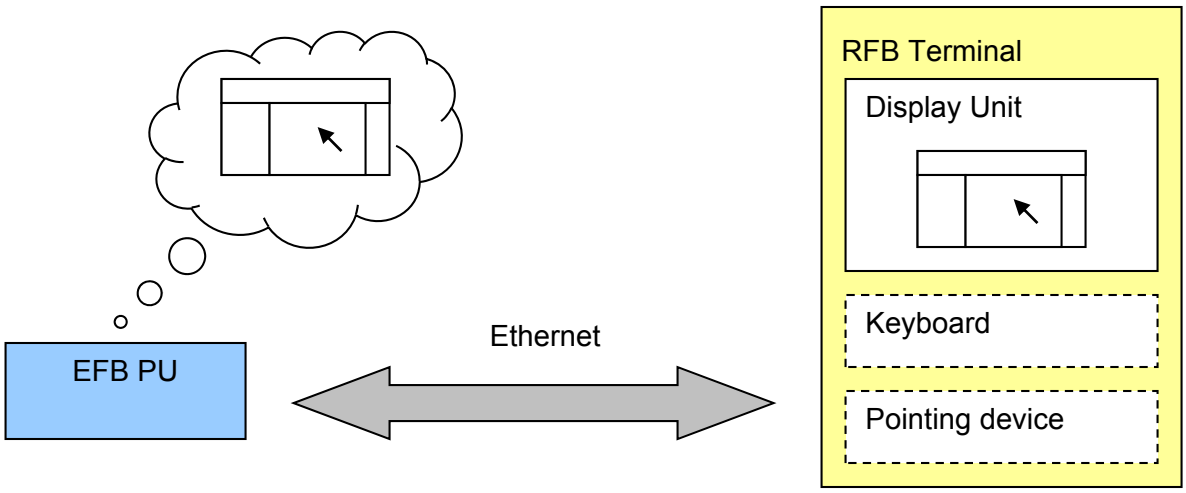


Figure L-1 – RFB Terminal Interface

L-1 Scope

This appendix defines:

- Remote Frame Buffer protocol that is used to display the screen of the EFB PU on a remote display unit and allowing control of the EFB PU with keyboard and/or pointing device (mouse, touch pad, touch screen etc.) events and
- Prerequisites and initialization steps required to use the remote display protocol.

L-2 Benefit

This standard is expected to minimize the overall cost of installing an EFB PU, a Terminal Unit, or both in the aircraft. In addition, it ensures full compatibility of EFB PUs and Terminals from different manufacturers.

L-3 Reference Documents

RFC 6143: Internet Engineering Task Force (IETF) Request for Comments: 6143, Category: Informational, ISSN: 2070-1721, published March 2011 (also known as the Remote Frame Buffer Protocol).

APPENDIX L
RFB TERMINAL INTERFACE

L-4 Definitions

Acronyms and terms uniquely associated with this appendix are described below.

AID – Aircraft Interface Device

DHCP – Dynamic Host Configuration Protocol

EFB – Electronic Flight Bag

EFB PU – EFB Processing Unit.

Part of a system (e.g., a part of an EFB) that consists of a processor, operating memory, possibly permanent data storage memory (e.g., a hard drive or a solid-state disk) and interface(s) required to interact with an Ethernet network (e.g., an Ethernet Network Adapter). It may consist of more parts, interfaces, and features (such as a local display unit) but these additional devices are not relevant in this context.

Ethernet

IEEE 802.3 computer networking standard

IP – Internet Protocol

NSU – Network Server Unit

Pointer

An input device controlling the mouse cursor or its equivalent. The function may be also provided by a touch screen, touch pad, or mouse.

RFB – Remote Frame Buffer

RFB terminal

A terminal that uses no standard video connections (such as analog VGA or digital LVDS or DVI) but receives the picture and transmits user input over an Ethernet connection (utilizing the RFB protocol). The RFB terminal is not limited to this function. Possible extensions (such as running local applications) are not covered by this document.

TCP – Transmission Control Protocol

APPENDIX L
RFB TERMINAL INTERFACE

L-5 Use Cases

A typical EFB use case includes an RFB terminal and an EFB PU. The actual implementation of physical connections is not covered by the specification. The following diagram is based on use case 2 in ARINC 828 Appendix C and is offered as an example only.

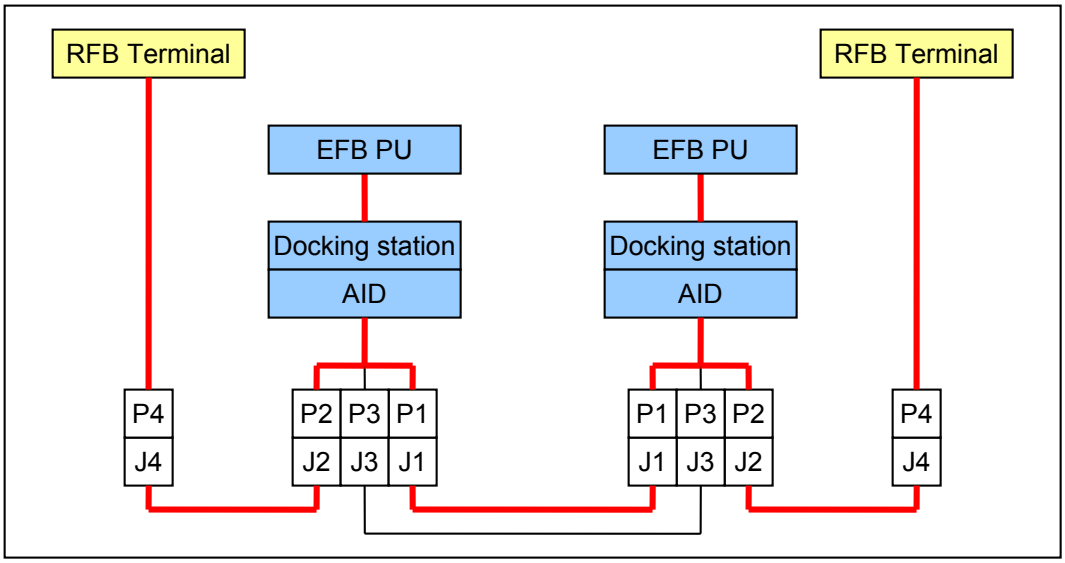


Figure L-2 – RFB Terminal Use Case

An RFB terminal has logical access to its local (own-site) and an off-site EFB PU. The RFB terminal implementation requires the ARINC 828 J2 and J4 connectors to support an Ethernet port.

Note: The LVDS/DVI wiring contained in the standard ARINC 828 J2 and J4 configuration is not required for the RFB implementation.

COMMENTARY

The display unit that is to be connected to a J4 receptacle must be compatible with the EFB PU (or AID) that is attached to the J2 receptacle. A mixed configuration (Ethernet on one unit and LVDS/DVI on the other) is not permitted.

APPENDIX L
RFB TERMINAL INTERFACE

L-6 Connector Usage

Data will be transferred using Ethernet and the RFB protocol. The standard configuration (as defined in Section 4.0) for ARINC 828 J2 and J4 connectors does not contain any Ethernet signals. Two quadrax contacts in J2 and J4 which were originally intended for LVDS signals per Tables 4.2 and 4.4 respectively will be used for Ethernet.

COMMENTARY

This signal reassignment is acceptable for retrofit applications where cabling has been previously installed, since LVDS and Ethernet require the same 100-ohm cable impedance.

Ethernet pin assignments are shown in Table L-1 and L-2 respectively for the J2 and J4 connectors. For installations using the “Alternate J4A” pin assignments (per Appendix H) Ethernet pin assignments are shown in Table L-3.

This interface may be supported using: 10Base-T, 100Base-TX, or 1000Base-T Ethernet. For 4-wire 10Base-T or 100Base_TX operation, only the first quadrax contact (Pin A) is used on the J2 and J4 connectors.

The signal name orientation (transmit versus receive) shown in tables L-1 thru L-3 refer the connected equipment assigned to that connector (J2, J4, J4A). E.g., J2 A-1 “Ethernet Transmit +” is the positive transmit output signal of the network adapter of the device connected to J2. Only the relevant signals on J2 and J4 are shown.

APPENDIX L
RFB TERMINAL INTERFACE

Table L-1 – Connector J2 pinout

Connector	Location	10Base-T and 100Base-TX		1000Base-T		Type
		Abbreviation	Description	Abbreviation	Description	
J2	A-1	ETH 1_TX+	Ethernet Transmit +	ETH 1_BI_DA+	Ethernet Bidirectional pair A+	Quadrax
J2	A-2	ETH 1_RX+	Ethernet Receive +	ETH 1_BI_DB+	Ethernet Bidirectional pair B+	
J2	A-3	ETH 1_TX-	Ethernet Transmit -	ETH 1_BI_DA-	Ethernet Bidirectional pair A-	
J2	A-4	ETH 1_RX-	Ethernet Receive -	ETH 1_BI_DB-	Ethernet Bidirectional pair B-	
J2	A-S	ETH 1_SH	Ethernet Shield	ETH 1_SH	Ethernet Shield	
J2	D-1	unused	unused	ETH 1_BI_DC+	Ethernet Bidirectional pair C+	
J2	D-2	unused	unused	ETH 1_BI_DD+	Ethernet Bidirectional pair D+	
J2	D-3	unused	unused	ETH 1_BI_DC-	Ethernet Bidirectional pair C-	
J2	D-4	unused	unused	ETH 1_BI_DD-	Ethernet Bidirectional pair D-	
J2	D-S	unused	unused	ETH 1_SH	Ethernet Shield	

COMMENTARY

For J4 installations (per Table 4-2) a straight wired cable is required between J2 and J4 (e.g., J2 A-1 wired to J4 A-1; J2 A-2 wired to J4 A-2; etc.).

For J4A installations (per Appendix H) a crossover wired cable is required between J2 and J4A (e.g., J2 A-1 wired to J4A A-2; J2 A-2 wired to J4A A-1; etc.).

APPENDIX L
RFB TERMINAL INTERFACE

Table L-2 – Connector J4 pinout

Connector	Location	10Base-T and 100Base-TX		1000Base-T		Type
		Abbreviation	Description	Abbreviation	Description	
J4	A-1	ETH 1_RX+	Ethernet Receive +	ETH 1_BI_DB+	Ethernet Bidirectional pair B+	Quadrax
J4	A-2	ETH 1_TX+	Ethernet Transmit +	ETH 1_BI_DA+	Ethernet Bidirectional pair A+	
J4	A-3	ETH 1_RX-	Ethernet Receive -	ETH 1_BI_DB-	Ethernet Bidirectional pair B-	
J4	A-4	ETH 1_TX-	Ethernet Transmit -	ETH 1_BI_DA-	Ethernet Bidirectional pair A-	
J4	A-S	ETH 1_SH	Ethernet Shield	ETH 1_SH	Ethernet Shield	
J4	D-1	unused	unused	ETH 1_BI_DD+	Ethernet Bidirectional pair D+	
J4	D-2	unused	unused	ETH 1_BI_DC+	Ethernet Bidirectional pair C+	
J4	D-3	unused	unused	ETH 1_BI_DD-	Ethernet Bidirectional pair D-	
J4	D-4	unused	unused	ETH 1_BI_DC-	Ethernet Bidirectional pair C-	
J4	D-S	unused	unused	ETH 1_SH	Ethernet Shield	

COMMENTARY

For J4 installations (per Table 4-2) a straight wired cable is required between J2 and J4 (e.g., J2 A-1 wired to J4 A-1; J2 A-2 wired to J4 A-2; etc.).

For J4A installations (per Appendix H) a crossover wired cable is required between J2 and J4A (e.g., J2 A-1 wired to J4A A-2; J2 A-2 wired to J4A A-1; etc.).

APPENDIX L
RFB TERMINAL INTERFACE

Table L-3 – Connector J4A pinout

Connector	Location	10Base-T and 100Base-TX		1000Base-T		Type
		Abbreviation	Description	Abbreviation	Description	
J4A	A-2	ETH 1_RX+	Ethernet Receive +	ETH 1_BI_DB+	Ethernet Bidirectional pair B+	Quadrax
J4A	A-1	ETH 1_TX+	Ethernet Transmit +	ETH 1_BI_DA+	Ethernet Bidirectional pair A+	
J4A	A-4	ETH 1_RX-	Ethernet Receive -	ETH 1_BI_DB-	Ethernet Bidirectional pair B-	
J4A	A-3	ETH 1_TX-	Ethernet Transmit -	ETH 1_BI_DA-	Ethernet Bidirectional pair A-	
J4A	A-S	ETH 1_SH	Ethernet Shield	ETH 1_SH	Ethernet Shield	
J4A	D-2	unused	unused	ETH 1_BI_DD+	Ethernet Bidirectional pair D+	
J4A	D-1	unused	unused	ETH 1_BI_DC+	Ethernet Bidirectional pair C+	
J4A	D-4	unused	unused	ETH 1_BI_DD-	Ethernet Bidirectional pair D-	
J4A	D-3	unused	unused	ETH 1_BI_DC-	Ethernet Bidirectional pair C-	
J4A	D-S	unused	unused	ETH 1_SH	Ethernet Shield	

COMMENTARY

For J4 installations (per Table 4-2) a straight wired cable is required between J2 and J4 (e.g., J2 A-1 wired to J4 A-1; J2 A-2 wired to J4 A-2; etc.).

For J4A installations (per Appendix H) a crossover wired cable is required between J2 and J4A (e.g., J2 A-1 wired to J4A A-2; J2 A-2 wired to J4A A-1; etc.).

APPENDIX L
RFB TERMINAL INTERFACE

L-7 IP Addressing

Depending on the actual network topology in the aircraft, the EFB PUs and Terminals may be attached to the same logical network domain or to a separate network domain, between which a router provides connectivity.

The terminals must be able to reach the local EFB PU and optionally an off-site EFB PU, assuming a cross-video function is to be provided.

The actual addressing scheme is left to system integrators. The following issues must be taken into account when designing the solution:

- If the EFB PUs are interchangeable on a daily basis, it would be useful to provide a DHCP service automatically assigning correct IP addresses to the EFB PUs with regard to their current location (e.g., the left side EFB PU should always receive the same IP address and the right side should also, to avoid problems with Terminals reaching the correct device).
- If the EFB PUs are fixed in the aircraft, using a fixed addressing scheme could save costs by eliminating the DHCP server.
- Each EFB PU should be able to establish an IP connection to each EFB PU.
- Each Terminal should be able to establish an IP connection to each EFB PU.

If the RFB terminals get their IP addresses from a DHCP server, a DHCP domain separation must be introduced in some cases. The following diagrams illustrate some examples:

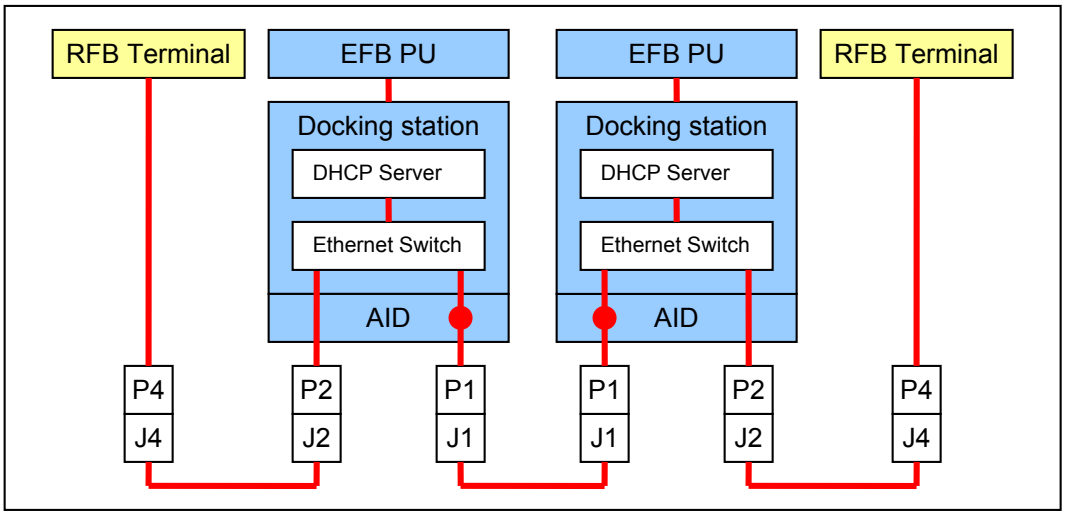


Figure L-3 – DHCP Server Example 1

- If a docking station contains a DHCP server assigning IP addresses to its own EFB PU and its own RFB terminal, the DHCP traffic must be blocked on the connection between the docking stations (depicted as a red dot on the connection between a docking station and a P1 socket).

APPENDIX L
RFB TERMINAL INTERFACE

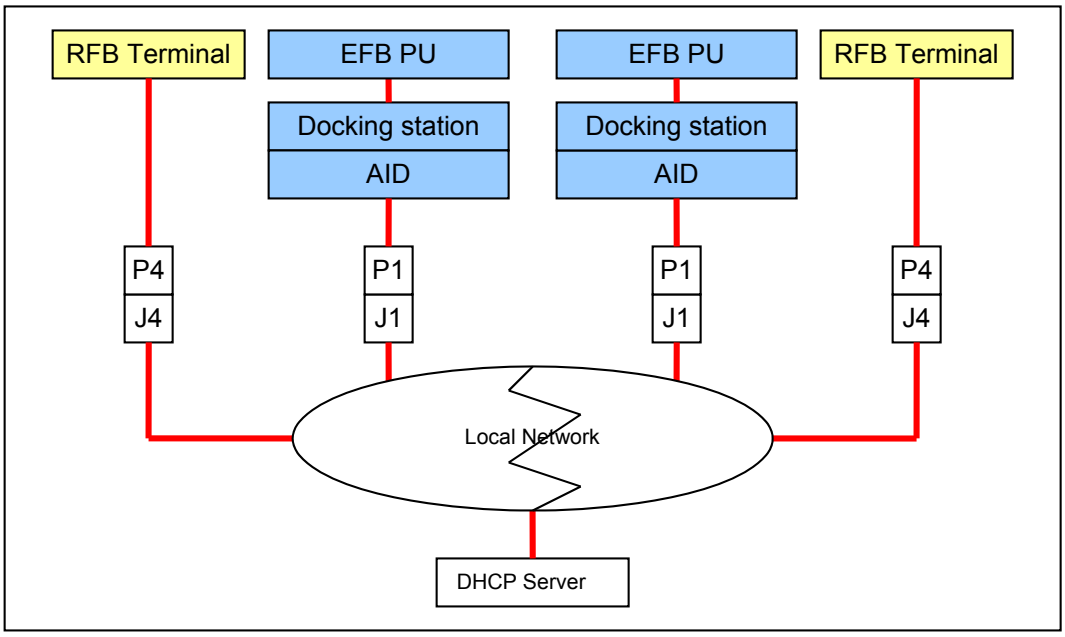


Figure L-4 – DHCP Server Example 2

- If a DHCP server is located in the local network, the DHCP server must be aware which segment requests an IP address assignment or traffic separation within the network must be implemented.

If the aircraft network addressing is not restricted by any existing solutions, it is suggested to use IP addresses from a private addressing space, e.g., 192.168.x.y/24.

It is recommended that RFB terminals and EFB PUs run IPv6-aware RFB client and server applications respectively.

L-8 Protocol RFB Terminal Interface

The protocol for accessing the EFB PU remotely is defined by RFC 6143 under the name Remote Framebuffer Protocol:

“RFB ("remote framebuffer") is a simple protocol for remote access to graphical user interfaces that allows a client to view and control a window system on another computer. Because it works at the framebuffer level, RFB is applicable to all windowing systems and applications.”

The Remote Framebuffer Protocol (as defined by RFC 6143) is the minimum which shall be supported by all implementations of terminals and EFB PUs to maintain compatibility. There are numerous implementations available for software and hardware platforms.

APPENDIX L
RFB TERMINAL INTERFACE

L-9 RFB Server in the EFB PU

The RFB server is a computer which actually drives the graphical user interface. The server draws all graphics, reacts to user input, and performs logic operations. The server allows clients to connect and transmit the video signal and user input over a computer network.

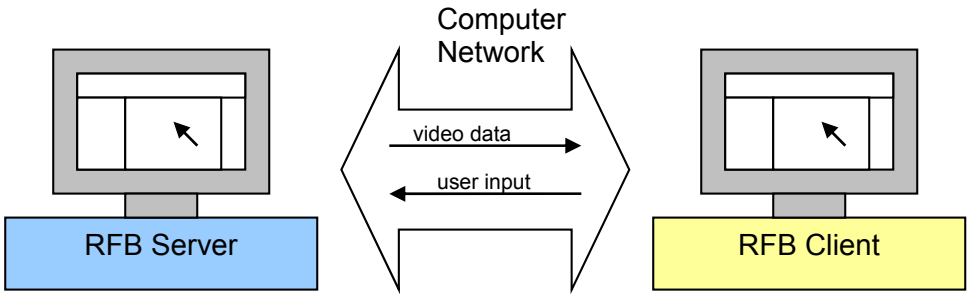


Figure L-5 – RFB Server Local Display

The server does not actually need a local display. It is enough that the graphical user interface exists virtually in its memory.

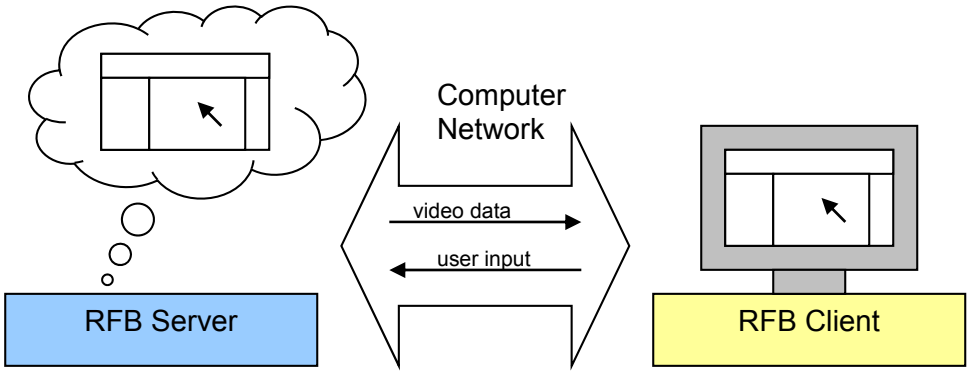


Figure L-6 – RFB Server in Virtual Memory

In all cases the role of the RFB server is fulfilled by an EFB PU.

L-10 RFB Client in the RFB Terminal

The RFB client is a thin-client in the client-server architecture. Its minimal functionality is to establish a network connection to an RFB server and show the remote display on its local display. Its functionality, however, is not limited and may include inter alia the following features:

- User input (pointer and/or keyboard)
- Selection of a remote server (one terminal for accessing multiple remote computers)
- Locally hosted additional software

The role of the RFB client is fulfilled by an RFB terminal. In addition, each EFB PU may also implement a client function in order to provide tunnelled connectivity to other systems. An example use case would be to offer a cross-video function for

installations without a logical cross-connectivity between an RFB terminal and an off-side EFB PU.

L-11 RFB Terminal

In the smart terminal approach, the logic is clearly separated and located only on the EFB PUs. The terminals are capable of establishing an RFB connection to their local EFB PUs and optionally to off-side EFB PUs in order to achieve a cross-video function.

The complete RFB client software is located and running within terminal's hardware. The cross-video function is realized within terminal's software and from outside is visible as different network connections.

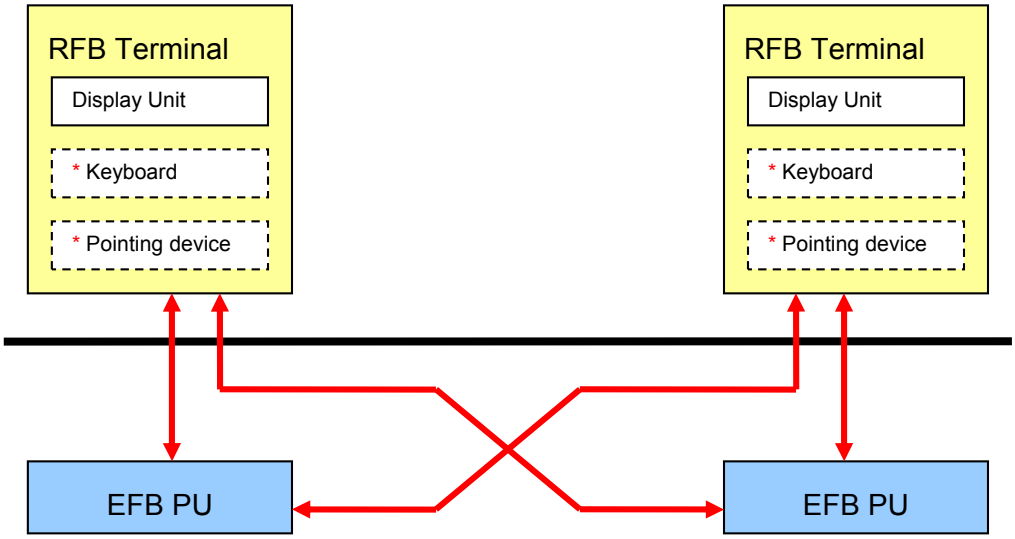


Figure L-7 – RFB Terminal Cross-Video Function

* At least one input device for each RFB terminal is mandatory.

Another possible variation is to make the terminal's software dynamic and load it from the EFB PU during initialization. Such an approach would give much more flexibility in customizing functions of the terminal:

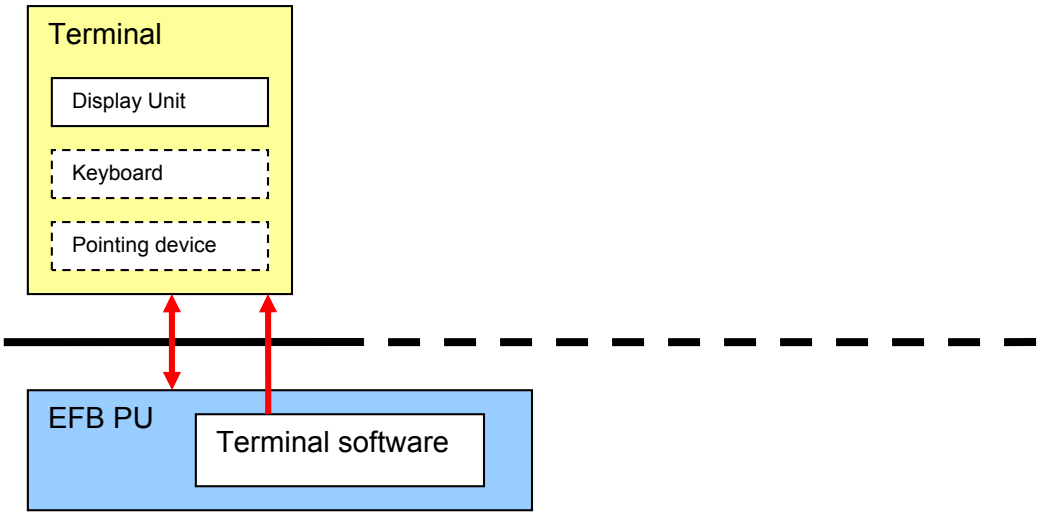


Figure L-8 – RFB Termional Dynamic Software

For details on offering terminal's software from the EFB PU, see Section L-22: *Dynamic RFB terminal's software*.

L-12 The EFB PU as a Terminal

It is possible to keep only one single network connection between a smart terminal and its local EFB PU, and realize the cross-video function within EFB PU's software:

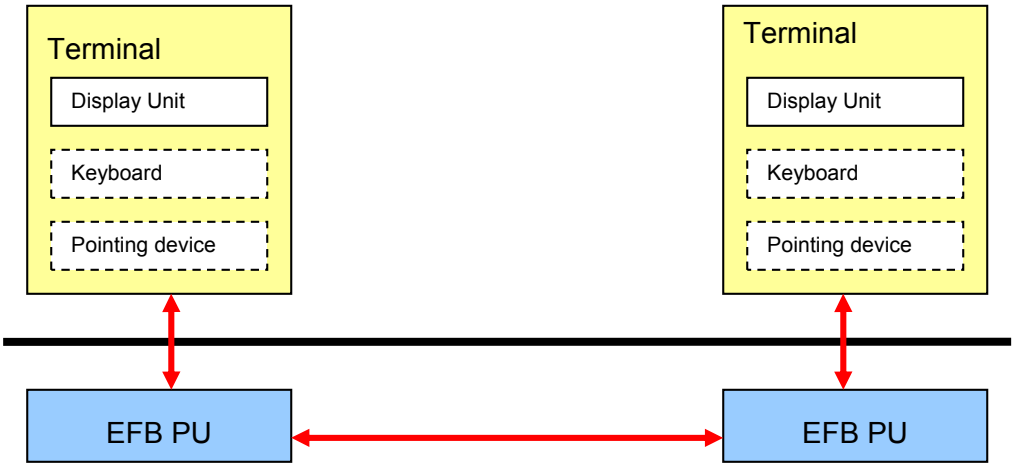


Figure L-9 – EFB PU Single Network Connection

In such an architecture, the following chain of events takes place when showing an off-side display:

- A local terminal connects to its local EFB PU and shows the display of the local EFB PU
- A local EFB PU connects to an off-side EFB PU and shows on its virtual display the display of the off-side EFB PU
- The consequence is that on the local terminal the off-side display is shown

There are two possible approaches to toggle the cross-video function:

- either sends the terminal a defined request to its own EFB PU, so that it knows that it should forward the off-side display (see Section L-21 – Cross-Video Request), or
- offers the EFB PU a local software function triggering the cross-video function (e.g., a dedicated icon on the EFB PU's menu bar)

A simpler variation of the approach is to reduce the smart terminal to a standard display and an input device:

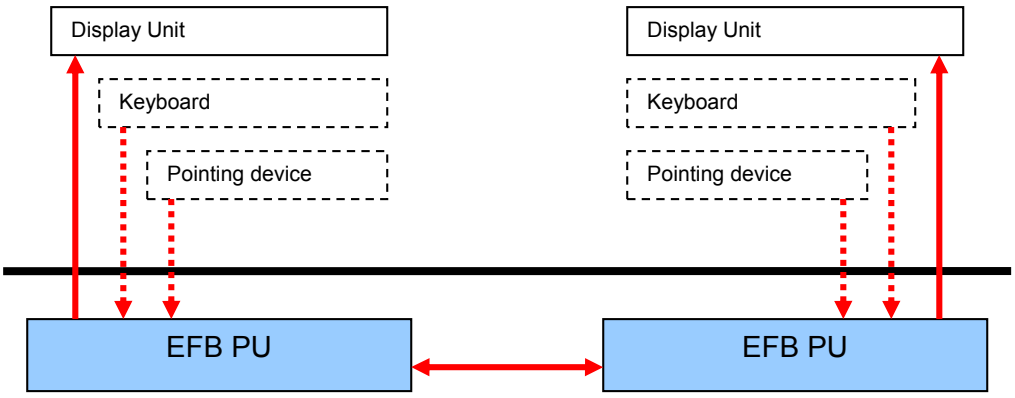


Figure L-10 – EFB PU Standard Display

Then the only RFB connection that may take place is between the EFB PUs for a cross-video function. There are still two possible approaches to toggle the cross-video function, as defined above.

L-13 Establishing an RFB Connection

The RFB client must be aware of network addressing in use and connect to an adequate RFB server for a local and a cross-video case. The actual addressing is out of the scope of this specification and is a matter of the system integration phase in the aircraft.

L-14 User Authentication

For fixed EFB PU installations (e.g., pure EFB Class 2 approach) it is recommended that no user authentication on an RFB client is required.

For floating EFB PU installations (e.g., dockable personalized EFB laptops) it is recommended to use other than RFB built-in security means (if required). Otherwise the following key issues must be considered by system integrators:

- the RFB credentials are defined by the RFB server (EFB PU); they are not necessarily equal to the credentials used by the operating system (or EFB software) that is running on the EFB PU
- only a few RFB client and server implementations are capable of using operating system's credentials for authorizing RFB connections
- if the EFB software uses a customized authentication process that is independent of the operating system's security layer, the RFB server is not capable of using such credentials for authorizing RFB connections
- a user does not necessarily have a keyboard; a terminal may need to offer an on-screen keyboard
- a thin-client does not necessarily support user authentication or does not necessarily support the same user authentication model as the one expected by the RFB server

L-15 Connection Encryption

The RFB protocol (as defined by RFC 6143) provides no security beyond the optional and cryptographically weak password check. Specifically, it provides no protection against observation of or tampering with the data stream.

However, as long as the RFB connection is established within a secure and separate cockpit network, there is no need for encrypting the data stream. Consequently, it is recommended that encryption mechanisms not be used, as they are not covered by the RFC 6143 standard.

If the cockpit network is shared with a passengers' network (or any other public-like network) the use of a strong encryption mechanism is a must. However, the topic is out of the scope of this specification and the actual technical solution is left to system integrators.

L-16 Default RFB Server Configuration

In order to provide maximum compatibility with a number of possible RFB client implementations, it is recommended to only use those features specified by the RFC 6143 standard.

Recommended default values for the available settings are defined in the table below:

Table L-3 – Default RFB Server Configuration

Parameter	Value	Description
IdleTimeout	0	The server shall not disconnect an idle session. A session is idle when a TCP connection between the server and the client still exists, but the client did not request any action (mouse pointer movement, mouse click event, keyboard input) for a long period of time.
AlwaysShared	1	The server shall allow multiple clients to be connected simultaneously. By prohibiting this feature a cross-video function may not be feasible (depending on solution).
UserPasswdVerifier	None	This specification assumes there are other than RFB built-in security means in use, so that the internal password verification can be always switched off. This value is provided as a recommendation.

L-17 Default RFB Client Configuration

In order to provide maximum compatibility with a number of possible RFB server implementations, it is recommended that only those features specified by the RFC-6143 standard be used.

Recommended default values for the available settings are defined in the table below:

Table L-4 – Default RFB Client Configuration

Parameter	Value	Description
UseLocalCursor	0	The remote server should generate the mouse pointer, if any. Any local cursor would interfere with intentions of application with showing and hiding the mouse cursor.
Shared	1	The client shall not request an exclusive session, as it would block potential cross-video sessions from another terminal (assuming the server would honor this request).
SendPtrEvents	1 for local 0 for off-side	A local terminal shall send mouse events to the server, while an off-side terminal should not.
SendKeyEvents	1 for local 0 for off-side	A local terminal shall send keyboard events (if a keyboard device is available), while an off-side terminal should not.
MenuKey	None	Some implementations of an RFB client show their local menus and/or settings toolbars by pressing a specific key or key combination. This should be avoided, so that most of possible keys and key combinations are redirected to the server.

L-18 Mirror Driver for Performance Improvement

As a price for being flexible (virtually any type of a display can be accessed over a network connection) the RFB protocol is not as efficient as solutions that understand the underlying graphic layout (e.g., X11 or RDP). The RFB protocol is pixel based

and the server needs some means to determine which parts of the display and how often to send to a client. These means can be optimized so that even a middle-resolution middle frame-rate movie can be transmitted.

In order to achieve such optimization, a mirror driver has to be installed in most of operating systems that offer RFB server functionality.

The mirror driver is neither specified in this document, nor by the RFC 6143 standard. This is an additional improvement of the RFB server's implementation, having nothing to do with the actual network protocol.

L-19 User Input

Each RFB client shall forward most possible user input and each RFB server shall accept most possible user input.

The matrix of accepted user inputs is presented below:

Table L-5 – Accepted User Inputs

	RFB client (local side)	RFB client (off-side)	RFB server (side independent)
Mouse position input	Yes*	No	Yes
Mouse left-button input	Yes*	No	Yes
Mouse right-button input	Yes*	No	Yes
Mouse additional buttons and scroll input	Optional*	No	Optional
Keyboard input	Yes*	No	Yes

* As far as the actual hardware configuration allows the input to be generated.

It is not recommended to:

- block any key or key-combination inputs that a standard PC US-layout keyboard offers (see Section L-21 – Cross-Video Request)
- block double (or multiple) click events

It is absolutely required to accept the following events as a minimum:

- mouse position change
- left mouse button click
- 0-9 key events from an alphanumeric keyboard
- A-Z key events
- Space and Shift key events
- exclamation mark, double-quotes, dollar symbol, percent symbol, ampersand symbol, slash symbol, backslash symbol, opening and closing parenthesis, equality sign, question mark, star symbol, plus and minus signs, apostrophe, hash symbol, comma, dot (full-stop), semicolon, colon and underline symbol key events

L-20 Mouse Pointer Synchronization

The RFB protocol transmits user interaction events in one direction only (from an RFB client to an RFB server). If the local mouse pointer of an RFB server is programmatically modified (position changed), the RFB client is not aware of this

fact. Depending on the RFB client configuration and available input devices the following situations may occur after encountering a mouse pointer desync followed by a mouse-click event generated by a user:

Table L-6 – Mouse Pointer Synchronization

	RFB terminal equipped with a relative pointing device (e.g., a mouse or a relative touch pad)	RFB terminal equipped with an absolute pointing device (e.g., a touch screen)
RFB client shows its own mouse pointer	(A) Two mouse pointers visible. Click event generated at possibly non-expected position (ambiguous).	(C) Two mouse pointers visible. Click event generated at an expected position.
RFB client does not show its own mouse pointer	(B) EFB PU's mouse pointer visible. Click event generated at a wrong position (= position of the RFB terminal's local invisible mouse position).	(D) EFB PU's mouse pointer visible. Click event generated at an expected position.

In order to solve the negative consequences of the cases (A) and (B), each EFB PU must inform all interested RFB terminals about the current position of its local mouse pointer, so that the RFB terminals can maintain synchronization.

L-21 Cross-Video Request

Basically, the cross-video function should be realized directly by the RFB clients simply by connecting to a local or to an off-side EFB.

While connected to a local EFB, the user-inputs shall be forwarded to the respective RFB server.

While connected to an off-side EFB, the user-inputs should be ignored, so that an off-side EFB state is not influenced.

If it is required that an RFB client performs a switch between the local and the off-side EFB by receiving a dedicated key event, then the following key combination is recommended:

Control + Alt + Num *

which generates the following virtual key sequence when pressed:

- 17 (for Control in general) or 162 (for Left-Control) or 163 (for Right-Control)
- 18 (for Alt in general) or 164 (for Left-Alt) or 165 (for Right-Alt)
- 106 (for Num *)

Please note that:

- the order of incoming Control and Alt events may be random
- the release key sequence does not necessarily contain all virtual keys and is not necessarily in the opposite order

APPENDIX L
RFB TERMINAL INTERFACE

L-22 Dynamic RFB Terminal's Software

It is possible that an RFB terminal does not contain any RFB client software, but loads it first during startup from a connected EFB and then executes.

In such an architecture, the EFB must provide a software package that can be accessed from an RFB terminal over network, loaded, and executed.

This feature is implementation dependent.

APPENDIX M ALTERNATE J1A CONNECTORS AND PIN ASSIGNMENTS

M-1 ALTERNATE J1A CONNECTOR AND PIN REQUIREMENTS

This appendix defines alternate pin assignments for specific Quadrax contact positions on the J1 connector. The following table identifies the affected contact positions:

Table M-1 – Contact Positions

Connector J1A
J1 - A

This Appendix refers to the alternate pin allocations for connector J1.

Contained in this Appendix is:

- J1A Connector Description by Location of Socket
- J1A Connector Description by Signal Function
- J1A Connector Termination Figure

APPENDIX M
ALTERNATE J1A CONNECTORS AND PIN ASSIGNMENTS

Table M-2 – J1A Connector Description by Location of Socket

<table>
<tr><th>Connector</th><th>Location</th><th>Abbrev</th><th>Description</th><th>Type</th></tr>
<tr><td>J1A</td><td>1</td><td>AC_DISC_GND</td><td>AC ground can be used for signal guard in pin allocation</td><td>#20</td></tr>
<tr><td>J1A</td><td>2</td><td>28VDC</td><td>28Vdc Power</td><td>#12</td></tr>
<tr><td>J1A</td><td>3</td><td>115VAC</td><td>115Vac Power</td><td>#12</td></tr>
<tr><td>J1A</td><td>4</td><td>EFB_DISC_GND</td><td>EFB ground can be used for signal guard in pin allocation</td><td>#20</td></tr>
<tr><td>J1A</td><td>5</td><td>28VDC_RTN</td><td>28Vdc_Return Power</td><td>#12</td></tr>
<tr><td>J1A</td><td>6</td><td>X_VIDEO_IN</td><td>Reserved for mfg assigned video function</td><td>#20</td></tr>
<tr><td>J1A</td><td>7</td><td>X_VIDEO_OUT</td><td>Reserved for mfg assigned video function</td><td>#20</td></tr>
<tr><td>J1A</td><td>A-1</td><td>10/100 ETH 5_TX+</td><td>Ethernet Transmit +</td><td>Quadrax</td></tr>
<tr><td>J1A</td><td>A-2</td><td>10/100 ETH 5_RX+</td><td>Ethernet Receive +</td><td>Quadrax</td></tr>
<tr><td>J1A</td><td>A-3</td><td>10/100 ETH 5_TX-</td><td>Ethernet Transmit -</td><td>Quadrax</td></tr>
<tr><td>J1A</td><td>A-4</td><td>10/100 ETH 5_RX-</td><td>Ethernet Receive -</td><td>Quadrax</td></tr>
<tr><td>J1A</td><td>A-S</td><td>ETH 5_SH</td><td>Ethernet Shield</td><td>Quadrax</td></tr>
<tr><td>J1A</td><td>B</td><td>EFB_DISC_2B</td><td>Device identification discrete for automatic device configuration
J1-B is Bit 1 (MSB)
where 0=gnd and 1=open
<table>
<tr><th>ID</th><th>MSB J1-B</th><th>LSB J1-Z</th></tr>
<tr><td>EFB_1</td><td>0</td><td>0</td></tr>
<tr><td>EFB_2</td><td>0</td><td>1</td></tr>
<tr><td>EFB_3</td><td>1</td><td>0</td></tr>
<tr><td>EFB_4 to n</td><td>1</td><td>1</td></tr>
</table></td><td>#20</td></tr>
<tr><td>J1A</td><td>C</td><td>AC_DISC_1</td><td>WOW (Air/Ground logic) weight on wheels</td><td>#16</td></tr>
<tr><td>J1A</td><td>D</td><td>AC_DISC_3</td><td>Reserved for mfg assigned function</td><td>#16</td></tr>
<tr><td>J1A</td><td>E</td><td>A717_1_RX+</td><td>ARINC 717 RX Data+</td><td>#16</td></tr>
<tr><td>J1A</td><td>F</td><td>A717_1_RX-</td><td>ARINC 717 RX Data-</td><td>#16</td></tr>
<tr><td>J1A</td><td>G</td><td>AC_DISC_GND</td><td>AC ground can be used for signal guard in pin allocation</td><td>#20</td></tr>
<tr><td rowspan="2">J1A</td><td rowspan="2">H-1</td><td>10/100 ETH 4_TX+</td><td rowspan="2">Ethernet Transmit +</td><td rowspan="2">Quadrax</td></tr>
<tr><td>1000 BI_DC+</td></tr>
<tr><td rowspan="2">J1A</td><td rowspan="2">H-2</td><td>10/100 ETH 4_RX+</td><td rowspan="2">Ethernet Receive +</td><td rowspan="2">Quadrax</td></tr>
<tr><td>1000 BI_DD+</td></tr>
<tr><td rowspan="2">J1A</td><td rowspan="2">H-3</td><td>10/100 ETH 4_TX-</td><td rowspan="2">Ethernet Transmit -</td><td rowspan="2">Quadrax</td></tr>
<tr><td>1000 BI_DC-</td></tr>
<tr><td rowspan="2">J1A</td><td rowspan="2">H-4</td><td>10/100 ETH 4_RX-</td><td rowspan="2">Ethernet Receive -</td><td rowspan="2">Quadrax</td></tr>
<tr><td>1000 BI_DD-</td></tr>
<tr><td>J1A</td><td>H-S</td><td>ETH 4_SH</td><td>Ethernet Shield</td><td>Quadrax</td></tr>
</table>

APPENDIX M
ALTERNATE J1A CONNECTORS AND PIN ASSIGNMENTS

Connector	Location	Abbrev	Description	Type
J1A	J	Chassis	Chassis Safety Ground	#16
J1A	K-1	10/100 ETH 1_TX+ 1000 BI_DA+	Ethernet Transmit +	Quadrax
J1A	K-2	10/100 ETH 1_RX+ 1000 BI_DB+	Ethernet Receive +	Quadrax
J1A	K-3	10/100 ETH 1_TX- 1000 BI_DA-	Ethernet Transmit -	Quadrax
J1A	K-4	10/100 ETH 1_RX- 1000 BI_DB-	Ethernet Receive -	Quadrax
J1A	K-S	ETH 1_SH	Ethernet Shield	Quadrax
J1A	L	EFB_DISC_GND	EFB ground can be used for signal guard in pin allocation	#20
J1A	M	EFB_DISC_3	Shutdown signal (On/Off)	#16
J1A	N	A429_1_RX-	ARINC 429 Receiver -	#16
J1A	P	A429_1_RX+	ARINC 429 Receiver +	#16
J1A	R	EFB_DISC_1	Reset	#16
J1A	S	EFB_DISC_5	Unit gets power from aircraft.	#20
J1A	T	AC_DISC_2	Aircraft AC/DC Power Available (to know if a certain bus is powered)	#16
J1A	U	AC_DISC_4	Reserved for mfg assigned function	#16
J1A	V	A717_1_RXSH	ARINC 717 RX Shield	#20
J1A	W	115VAC_RTN	115Vac Return Power	#12
J1A	X	EFB_DISC_4	Unit active	#20
J1A	Y	A429_1_RXSH	ARINC 429 RX Shield	#16
J1A	Z	EFB_DISC_2A	Device identification discrete for automatic device configuration J1-Z is Bit 0 (LSB) where 0=gnd and 1=open ID / MSB J1-B / LSB J1-Z EFB_1: 0 / 0 EFB_2: 0 / 1 EFB_3: 1 / 0 EFB_4 to n: 1 / 1	#16

APPENDIX M
ALTERNATE J1A CONNECTORS AND PIN ASSIGNMENTS

Table M-3 – J1A Connector Description by Signal Function

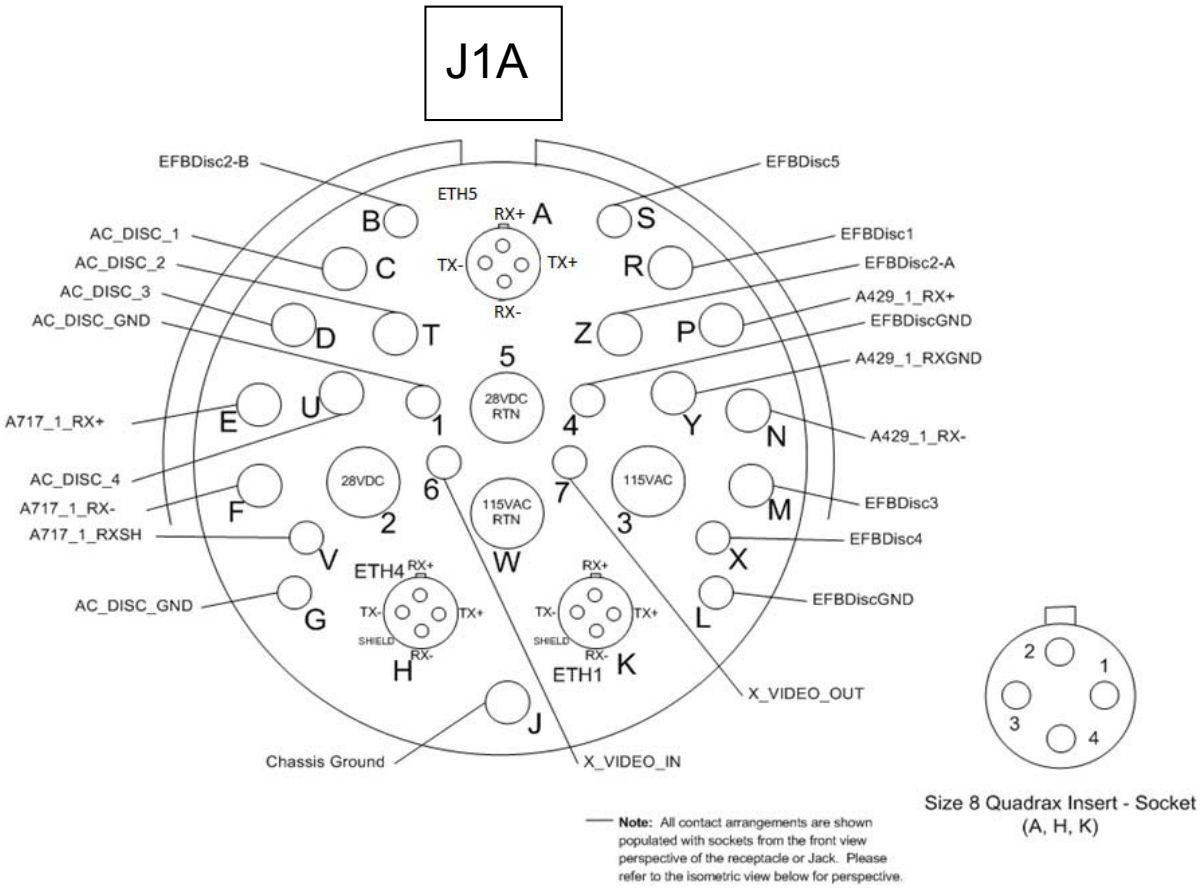
Connector	Location	Abbrev	Description	Type
J1A		A429_1	Most important avionics data	
J1A	P	A429_1_RX+	ARINC 429 Receiver +	#16
J1A	N	A429_1_RX-	ARINC 429 Receiver -	#16
J1A	Y	A429_1_RXSH	ARINC 429 RX Shield	#16
J1A		ARINC 717	ARINC 717 FDR/QAR Data Bus	
J1A	E	A717_1_RX+	ARINC 717 RX Data+	#16
J1A	F	A717_1_RX-	ARINC 717 RX Data-	#16
J1A	V	A717_1_RXSH	ARINC 717 RX Shield	#20
J1A	K	Ethernet #1 10/100/1000	Connected to aircraft installed switch or router	
J1A	K-1	10/100 ETH 1_TX+ 1000 BI_DA+	Ethernet Transmit +	Quadrax
J1A	K-3	10/100 ETH 1_TX- 1000 BI_DA-	Ethernet Transmit -	Quadrax
J1A	K-2	10/100 ETH 1_RX+ 1000 BI_DB+	Ethernet Receive +	Quadrax
J1A	K-4	10/100 ETH 1_RX- 1000 BI_DB-	Ethernet Receive -	Quadrax
J1A	K-S	ETH 1_SH	Ethernet Shield	Quadrax
J1A	H	Ethernet #4 10/100/1000	Connection intended for EFB-EFB Cross Over Functionality	
J1A	H-1	10/100 ETH 4_TX+ 1000 BI_DC+	Ethernet Transmit +	Quadrax
J1A	H-3	10/100 ETH 4_TX- 1000 BI_DC-	Ethernet Transmit -	Quadrax
J1A	H-2	10/100 ETH 4_RX+ 1000 BI_DD+	Ethernet Receive +	Quadrax
J1A	H-4	10/100 ETH 4_RX- 1000 BI_DD-	Ethernet Receive -	Quadrax
J1A	H-S	ETH 4_SH	Ethernet Shield	Quadrax
J1A		Ethernet #5 10/100	Connected to aircraft installed switch or router	
J1A	A-1	10/100 ETH 5_TX+	Ethernet Transmit +	Quadrax
J1A	A-3	10/100 ETH 5_TX-	Ethernet Transmit -	Quadrax
J1A	A-2	10/100 ETH 5_RX+	Ethernet Receive +	Quadrax
J1A	A-4	10/100 ETH 5_RX-	Ethernet Receive -	Quadrax
J1A	A-S	ETH 5_SH	Ethernet Shield	Quadrax
J1A		ACDisc1	WOW (Air/Ground logic) weight on wheels	
J1A	C	AC_DISC_1	WOW (Air/Ground logic) weight on wheels	#16
J1A		ACDisc2	Aircraft AC/DC Power Available (to know if a certain bus is powered)	
J1A	T	AC_DISC_2	Aircraft AC/DC Power Available (to know if a certain bus is powered)	#16
J1A		ACDisc3	Reserved for aircraft specific discrete	
J1A	D	AC_DISC_3	Reserved for mfg assigned function	#16
J1A		ACDisc4	Reserved for aircraft specific discrete	
J1A	U	AC_DISC_4	Reserved for mfg assigned function	#16
J1A		ACDisc Ground	Reserved for aircraft specific discrete	

APPENDIX M
ALTERNATE J1A CONNECTORS AND PIN ASSIGNMENTS

Connector	Location	Abbrev	Description	Type
J1A	1	AC_DISC_GND	AC ground can be used for signal guard in pin allocation	#20
J1A	G	AC_DISC_GND	AC ground can be used for signal guard in pin allocation	#20
J1A		EFB_Disc_1	Reset	
J1A	R	EFB_Disc_1	Reset	#16
J1A		EFBDisc2	Device identification discrete for automatic device configuration J1-B is Bit 1 (MSB) ID / MSB J1-B / LSB J1-Z CAPT / 0 / 0 FO / 0 / 1 EFB_3 / 1 / 0 EFB_4 to n / 1 / 1	
J1A	Z	EFB_DISC_2A	Device identification discrete for automatic device configuration J1-Z is Bit 0 (LSB)	#16
J1A	B	EFB_DISC_2B	Device identification discrete for automatic device configuration J1-B is Bit 1 (MSB)	#20
J1A		EFBDisc3	Shutdown signal (On/Off)	
J1A	M	EFB_DISC_3	Shutdown signal (On/Off)	#16
J1A		EFBDisc4	Unit active	
J1A	X	EFB_DISC_4	Unit active	#20
J1A		EFBDisc5	Unit gets power from aircraft	
J1A	S	EFB_DISC_5	Unit gets power from aircraft	#20
J1A		EFBDisc Ground	Unit gets power from aircraft	
J1A	4	EFB_DISC_GND	EFB ground can be used for signal guard in pin allocation	#20
J1A	L	EFB_DISC_GND	EFB ground can be used for signal guard in pin allocation	#20
J1A		AC Power	115Vac Power	
J1A	3	115VAC	115Vac Power	#12
J1A	W	115VAC_RTN	115Vac Return Power	#12
J1A	J	Chassis	Chassis Safety Ground	#16
J1A		DC Power	28Vdc Power	
J1A	2	28VDC	28Vdc Power	#12
J1A	5	28VDC_RTN	28Vdc_Return Power	#12
J1A		X_Video	Cross video discretes	
J1A	6	X_VIDEO_IN	reserved for mfg assigned video function	#20
J1A	7	X_VIDEO_OUT	reserved for mfg assigned video function	#20

APPENDIX M
ALTERNATE J1A CONNECTORS AND PIN ASSIGNMENTS

M-2 - J1A Connector Termination



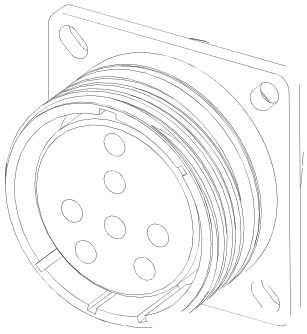


Figure B-1 – J1A: EN3645-F0JL20FA

APPENDIX N ALTERNATE J6 AND J7 CONNECTORS AND PIN REQUIREMENTS

This appendix defines connectors J6 and J7 are intended as a smaller alternative to connectors J1 - J4.

The references of these two connectors are:

- J6: EN3645M0AQ01FN
- J7: EN3645M0BN05FN (DC Power)
- J7: EN3645M0BN05FA (AC Power)

J7 Maxium Allowable Current is 7.5 Amps

Contained in this Appendix are:

- J6 and J7 Connector Description by Location of Socket
- J6 and J7 Connector Description by Signal Function
- J6 and J7 Connector Termination Figure

Table N-1 – J6 Connector Description by Location of Socket

Connector	Location	Abbrev	Description	Type
J6	A-1	10/100 ETH 6_TX+	Ethernet Transmit +	Quadrax
J6	A-2	10/100 ETH 6_RX+	Ethernet Receive +	Quadrax
J6	A-3	10/100 ETH 6_TX-	Ethernet Transmit -	Quadrax
J6	A-4	10/100 ETH 6_RX-	Ethernet Receive -	Quadrax
J6	A-S	ETH 6_SH	Ethernet Shield	Quadrax

Table N-2A – J7 Connector Description by Location of Socket AC Power

Connector	Location	Abbrev	Description	Type	Connector Keying
J7	A	115VAC	Power	#20	A
J7	B	115VAC_RTN	Return Power	#20	A
J7	C	Chassis GND	Chassis Safety Ground	#20	A
J7	D	DISC_1	Discrete	#20	A
J7	E	DISC_2	Discrete	#20	A

Table N-2B – J7 Connector Description by Location of Socket DC Power

Connector	Location	Abbrev	Description	Type	Connector Keying
J7	A	28VDC	Power	#20	N
J7	B	28VDC_RTN	Return Power	#20	N
J7	C	Chassis GND	Chassis Safety Ground	#20	N
J7	D	DISC_1	Discrete	#20	N
J7	E	DISC_2	Discrete	#20	N

APPENDIX N
Alternative J6 AND J7 CONNECTORS AND PIN REQUIREMENTS

Table N-3 – J6 Connector Description by Signal Function

Connector	Location	Abbrev	Description	Type
J6				
J6	A-1	10/100 ETH 6_TX+	Ethernet Transmit +	Quadrax
J6	A-2	10/100 ETH 6_RX+	Ethernet Receive +	Quadrax
J6	A-3	10/100 ETH 6_TX-	Ethernet Transmit -	Quadrax
J6	A-4	10/100 ETH 6_RX-	Ethernet Receive -	Quadrax
J6	A-S	ETH 6_SH	Ethernet Shield	Quadrax

Table N-4A – J7 Connector Description by Signal Function AC Power

Connector	Location	Abbrev	Description	Type	Connector Keying
J7	A	115VAC	Power	#20	A
J7	B	115VAC_RTN	Return Power	#20	A
J7	C	Chassis GND	Chassis Safety Ground	#20	A
J7	D	DISC_1	Discrete	#20	A
J7	E	DISC_2	Discrete	#20	A

Table N-4B – J7 Connector Description by Signal Function DC Power

Connector	Location	Abbrev	Description	Type	Connector Keying
J7	A	28VDC	Power	#20	N
J7	B	28VDC_RTN	Return Power	#20	N
J7	C	Chassis GND	Chassis Safety Ground	#20	N
J7	D	DISC_1	Discrete	#20	N
J7	E	DISC_2	Discrete	#20	N

APPENDIX N
Alternative J6 AND J7 CONNECTORS AND PIN REQUIREMENTS

CONNECTOR TERMINATION

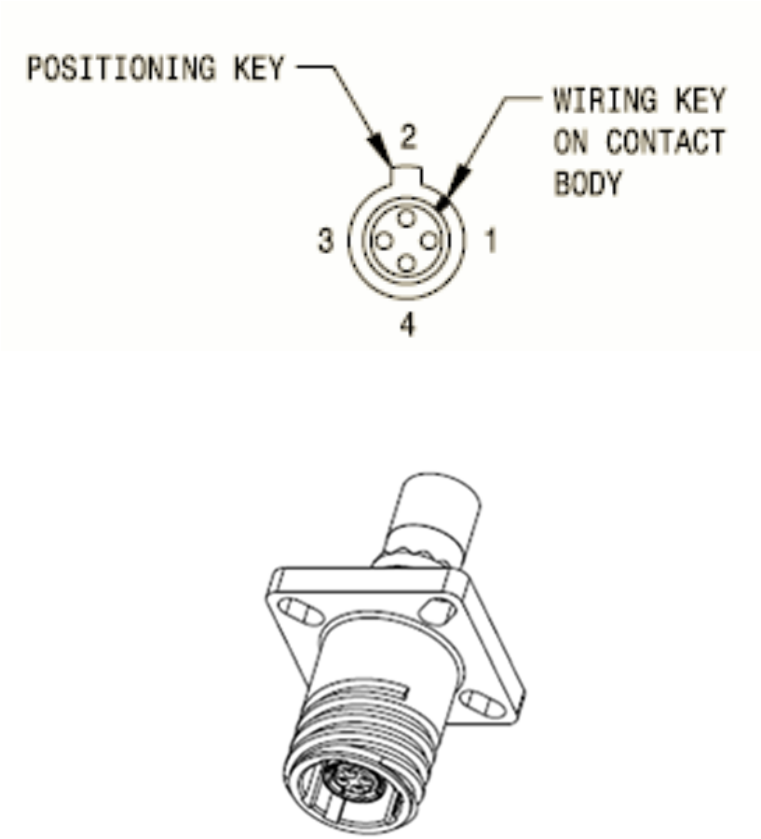
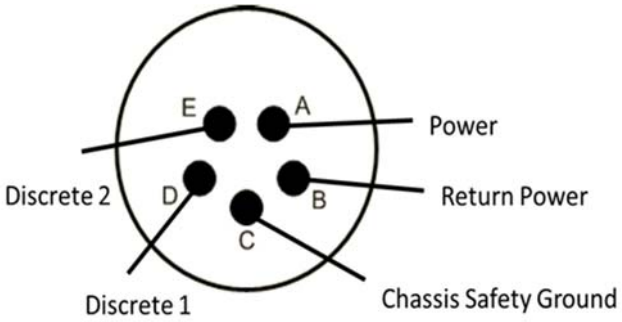


Figure N-1 – J6: EN3645M0AQ01FN

APPENDIX N
Alternative J6 AND J7 CONNECTORS AND PIN REQUIREMENTS

CONNECTOR TERMINATION



- Connector Keying A is for AC
- Connector Keying N is for DC

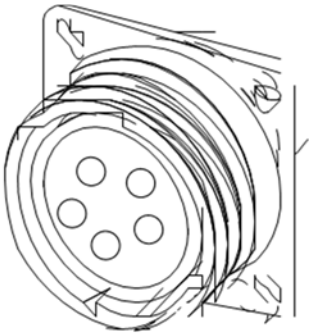


Figure N-2 – J7: EN3645M0BN05FA (AC Power)
J7: EN3645M0BN05FN (DC Power)