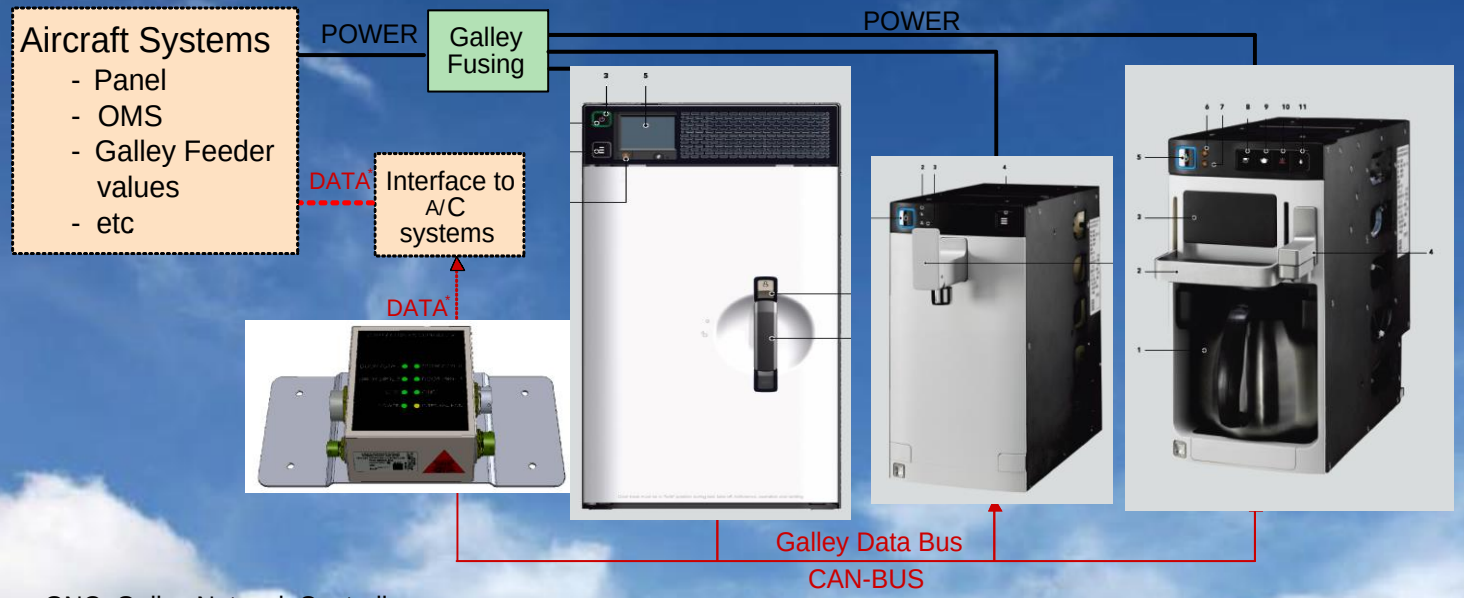
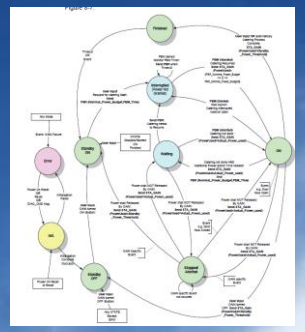


GNC: Galley Network Controller



AIRBUS Input 812A

Lessons Learned A350 implementation

→ Bit Timing and Sample Point Definition (ARINC 825)

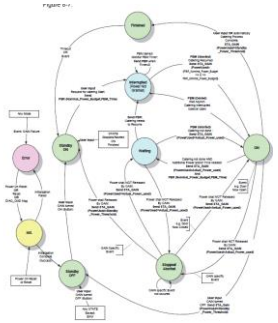
→ Oscillator Tolerance and Dependencies

Ralph Schnabel

February 20th, 2018

AIRBUS

A350XWB Lessons Learnt --- Bit Timing and Sample Point



History / Current as-is summary:

Decision has been made not to dublicate definitions from other leading project papers like e.g. ARINC825. However it has painfully been experienced that fundamental defintions have not been considered.

Therefore the proposal is to copy the following part out of ARINC825, but to add in the ARINC812 introduction part that the leading definiton Is still the original project paper. Similar approach has been conducted as connectors have been transfered to ARINC 625 (TBC)

Sample POINT

- The Sample Point location for all phases shall be 75% of the bit time.

CAN clock root frequency definiton:

- All CAN nodes on a bus should have the same CAN clock root frequency: either 20MHz, 40MHz, or 80MHz.

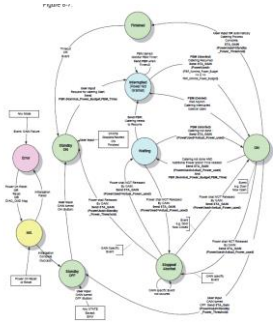
- **Classical CAN transceivers shall comply with ISO-11898-2: 2003 requirements.**
- **CAN FD transceivers shall comply with ISO-11898-2: 2016 requirements and asymmetries.**

BIT TIMING:

- **For Classical CAN and CAN FD arbitration, ARINC 825-bit timing parameters yield the following equations. The most constraining places the upper bound on the bit rate.** $Bit\ Rate\ Max$<0.287$Twire$+$TNode$+max($TRise$,$TFall$) $Bit\ Rate\ Max$<0.6052[$Twire$+$TNode$+max($TRise$,$TFall$)]+$Asym1$ $Bit\ Rate\ Max$<0.155$Asym2$ $Asym1$=$btReference$−min($tbit$(Bus))−min(Δ$tRec$) $Asym2$=max($tbit$(Bus))−$btReference$+max(Δ$tRec$)
- **For 2 Mbps transceiver, Asym1 = 130ns, Asym2 = 70ns; for 5 Mbps transceiver, Asym1 = 90ns, Asym2 = 25ns per ISO 11898-2: 2016. Max(TRise,TFall) corresponds to the worst case rise or fall time for the waveform.**

AIRBUS

A350XWB Lessons Learnt --- Bit Timing and Sample Point



Oscillator Tolerance:

Additional explanation / note shall be added to ARINC 812A

- NOTE:

Deviation in the oscillator from its stated value that can change slightly over time. If two oscillators were to deviate from the norm value by a significant amount and in opposite directions, there is the possibility that they would be unable to read each other's messages

- **Bit timing tolerance and oscillator tolerance result in a combined effect: skewing the relative edges of bits between multiple nodes. The SJW counters this effect but it must be set to provide enough margin. ARINC 825 is strict, compared to the automotive industry, in the allowable tolerances for oscillator and bit timing. While the automotive industry allowed 1% oscillator tolerances or more for Classical CAN and about 0.5% tolerance for CAN FD, ARINC 825 currently requires a 0.01% oscillator tolerance and 0.15% bit time tolerance over the life of the device. These combine to a 0.16% tolerance on the bit timing that can accumulate between rising edges over the different conditions defined above.**
- **The SJW, at a minimum, must accommodate this skew and, as can be seen in Figure I-3, could accommodate higher bit time tolerances than allowed in ARINC 825 even for very high data rates.**
- **Given the analysis above and the data rate limitations imposed by CAN implementations in avionics, it is proposed that an oscillator tolerance of 0.05% is well within acceptable bounds and enables cost reduction for LRU. The SJW required for this worst-case tolerance over the life of the unit (0.2% of a bit time total, combining 0.15% and 0.05% allowable) is approximately 1/16 of a bit time**

AIRBUS

Thank you

AIRBUS